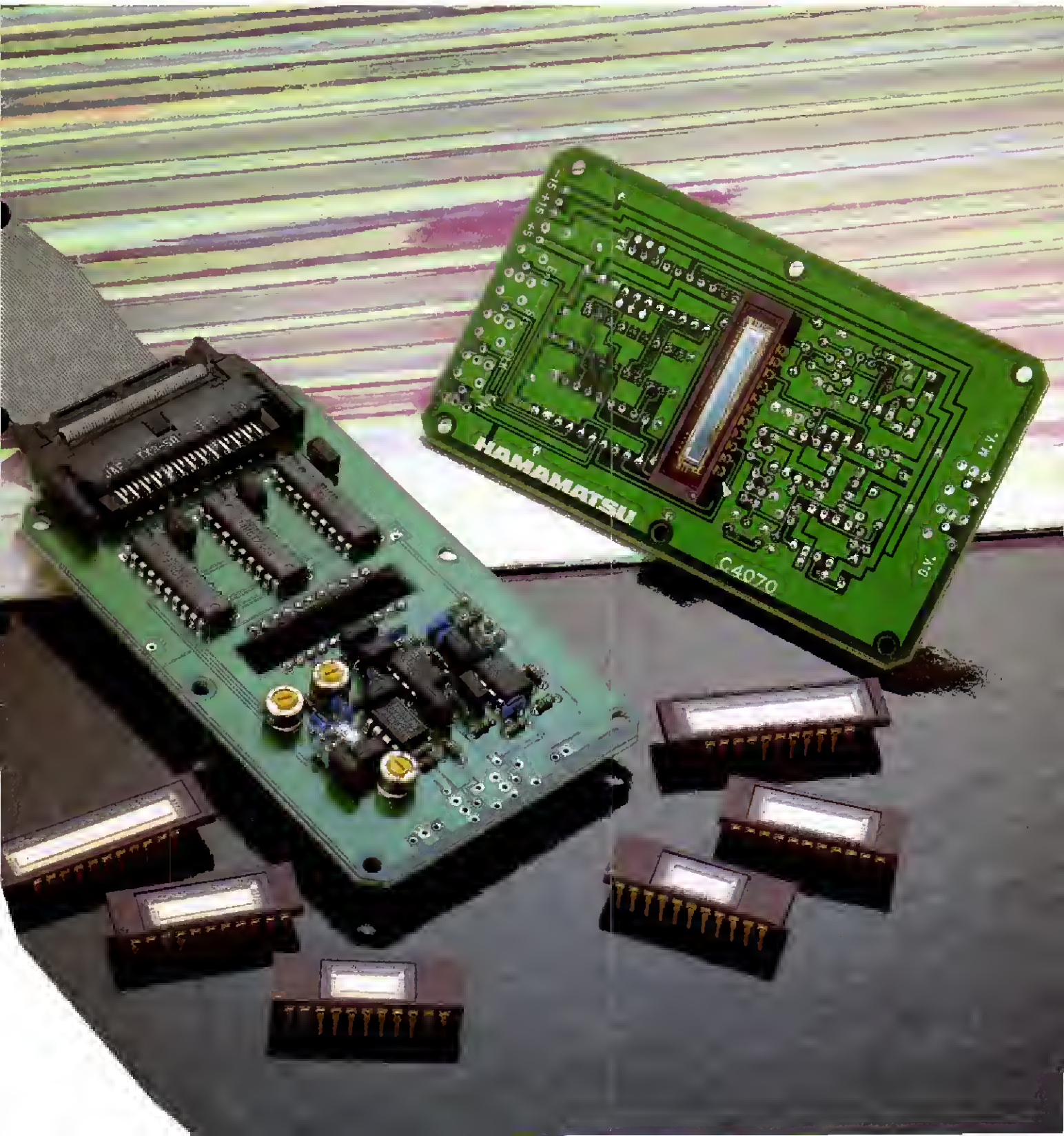
HAMAMATSU

MOS Linear Image Sensors

1990 CATALOG



SELECTION GUIDE

Type No.	Number of Photodiodes	Sensitive Area per Element (Photodiode Pitch × Height)	Total Sensitive Area	Spectral Response	Distinct Features	Page
Serial/Current Output Types						
S3901-128Q	128	50μm × 2.5mm	6.4 × 2.5mm	200 to 1000nm	• Low power consumption • Superior linearity • Wide dynamic range	1
-256Q	256		12.8 × 2.5mm			
-512Q	512		25.6 × 2.5mm			
S3904-256Q	256	25μm × 2.5mm	6.4 × 2.5mm	200 to 1000nm		
-512Q	512		12.8 × 2.5mm			
-1024Q	1024		25.6 × 2.5mm			
S3902-128Q	128	50μm × 0.5mm	6.4 × 0.5mm	200 to 1000nm		9
-256Q	256		12.8 × 0.5mm			
-512Q	512		25.6 × 0.5mm			
S3903-256Q	256	25μm × 0.5mm	6.4 × 0.5mm	200 to 1000nm		
-512Q	512		12.8 × 0.5mm			
-1024Q	1024		25.6 × 0.5mm			
Serial/Voltage Output Types						
S3921-128Q	128	50μm × 2.5mm	6.4 × 2.5mm	200 to 1000nm	• Boxcar output waveform • Simple external readout circuit • Wide dynamic range	17
-256Q	256		12.8 × 2.5mm			
-512Q	512		25.6 × 2.5mm			
S3924-256Q	256	25μm × 2.5mm	6.4 × 2.5mm	200 to 1000nm		
-512Q	512		12.8 × 2.5mm			
-1024Q	1024		25.6 × 2.5mm			
S3922-128Q	128	50μm × 0.5mm	6.4 × 0.5mm	200 to 1000nm		25
-256Q	256		12.8 × 0.5mm			
-512Q	512		25.6 × 0.5mm			
S3923-256Q	256	25μm × 0.5mm	6.4 × 0.5mm	200 to 1000nm		
-512Q	512		12.8 × 0.5mm			
-1024Q	1024		25.6 × 0.5mm			
Random Address Types						
S3900-512Q	512	25μm × 2.5mm	12.8 × 2.5mm	200 to 1000nm	• Random address readout • Current output	33
-1024Q	1024		25.6 × 2.5mm			
S3906-512Q	512	25μm × 0.5mm	12.8 × 0.5mm	200 to 1000nm		
-1024Q	1024		25.6 × 0.5mm			

Peripheral Circuits (Driver/Amplifier Circuits and Pulse Generators)

Type No.	Applicable MOS Linear Image Sensors	Features	Page
C4069	S3901, S3902, S3903, S3904	High speed operation	41
C4070	S3901, S3902, S3903, S3904	Low noise operation, superior linearity, boxcar output waveform	43
C4072	S3900, S3906	Low noise operation, superior linearity, boxcar output waveform	45
C4074	S3921, S3922, S3923, S3924	Simple construction, boxcar output waveform, low cost	47
C4091	Pulse generator for C4069, C4070, and C4074		

In addition to the extensive range of standard devices, Hamamatsu will design and manufacture custom image sensors and peripheral circuits, such as image sensors with fiber optic faceplates, special packages, or integrated signal processing circuitry. Hamamatsu welcomes your special requirements.

HAMAMATSU

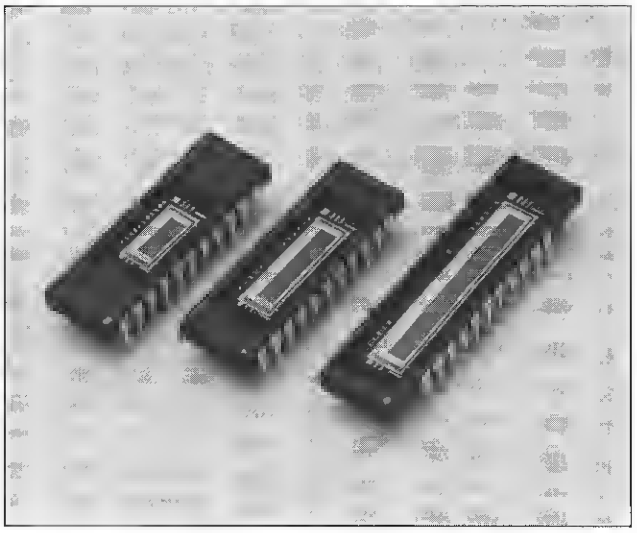
TECHNICAL DATA

SERIAL/CURRENT OUTPUT TYPE MOS LINEAR IMAGE SENSORS S3901, S3904 SERIES

Wide Sensitive Area (2.5mm Photodiode Height), High UV Sensitivity, Excellent Photometric Capabilities, Low Power Consumption

FEATURES

- **Wide photosensitive area**
  Photodiode pitch : 50μm (S3901), 25μm (S3904)
  Photodiode height : 2.5mm
- **High UV sensitivity with good stability**
- **Excellent photometric capabilities**
  Low dark current and high saturation charge
  Good linearity
  Wide dynamic range
- **Low power consumption : less than 1mW**
- **Start pulse and clock pulses are CMOS logic compatible**



APPLICATIONS

- **Multichannel spectrophotometry**
- **Image readout systems**

DESCRIPTION

By applying NMOS technology to the manufacture of self-scanning linear photodiode arrays, Hamamatsu can offer higher performance and increased flexibility to photometric instrument manufacturers. The new design achieves high UV sensitivity without deterioration even by extended UV exposure. Application is simplified because of low power consumption and single video output line. All members of the series are pin compatible.

The S3901 and S3904 series MOS linear image sensors feature a good output linearity over a wide dynamic range and low power consumption, and have a wide photosensitive area of 2.5mm photodiode height with a photodiode pitch of 50μm (S3901) or 25μm (S3904). Each series is available with three different number of photodiodes; 128, 256 and 512 for the S3901 series, 256, 512 and 1024 for the S3904 series.

Figure 1: Equivalent Circuit

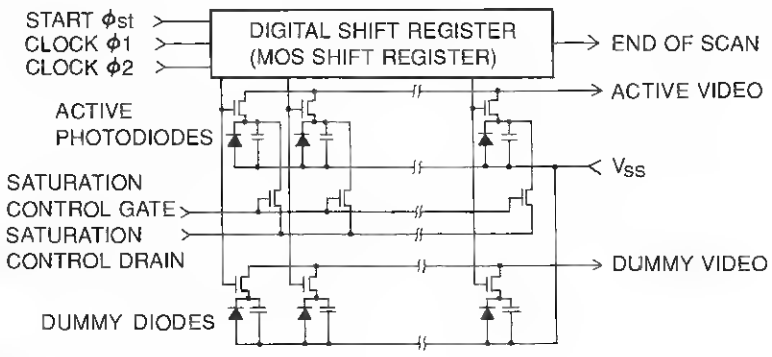
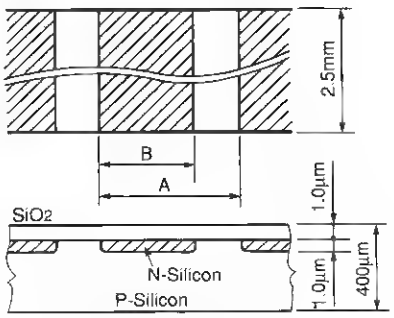


Figure 2: Sensor Geometry



S3901: A=50μm, B=45μm
S3904: A=25μm, B=20μm

MAXIMUM RATINGS

Parameters	Symbols	S3901, S3904 Series	Units
Supply Clock Amplitude	V_ϕ	15	V
Qperating Temperature ①	Topr	−40 to +65	°C
Storage Temperature	Tstg	−40 to +85	°C

① No dew

ELECTRICAL CHARACTERISTICS (Ta=25°C)

Parameters	Symbols	S3901 Series			S3904 Series			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Video Bias Voltage ①	V_b	1.5	V_ϕ−3.0	V_ϕ−2.5	1.5	V_ϕ−3.0	V_ϕ−2.5	V
Saturation Control Gate Voltage	V_{scg}	—	0	—	—	0	—	V
Saturation Control Drain Voltage	V_{scd}	—	V_b	—	—	V_b	—	V
Start Pulse Voltage (ϕst) ① -High	$V_{\phi s}$(H)	4.5	V_ϕ	10	4.5	V_ϕ	10	V
-Low	$V_{\phi s}$(L)	0	—	0.4	0	—	0.4	V
Clock Pulse Voltage (ϕ1, ϕ2) -High	Vϕ1, Vϕ2(H)	4.5	5	10	4.5	5	10	V
-Low	Vϕ1, Vϕ2(L)	0	—	0.4	0	—	0.4	V
Start Pulse Rise/Fall Times (ϕst)	$t_{r\phi s}$, $t_{f\phi s}$	—	—	500	—	—	500	ns
Start Pulsewidth (ϕst)	$t_{pw\phi s}$	200	—	—	200	—	—	ns
Clock Pulse Rise/Fall Times (ϕ1, ϕ2)	$t_{r\phi 1}$, $t_{r\phi 2}$, $t_{f\phi 1}$, $t_{f\phi 2}$	—	—	500	—	—	500	ns
Clock Pulsewidth (ϕ1, ϕ2)	$t_{pw\phi 1}$, $t_{pw\phi 2}$	200	—	—	200	—	—	ns
Start Pulse (ϕst) and Clock Pulse (ϕ2) Qverlap	$t_{\phi ov}$	200	—	—	200	—	—	ns
Clock Pulse Space	X_1, X_2	0	—	—	0	—	—	ns
Data Rate	f	0.1	—	2000	0.1	—	2000	kHz
Video Delay Time (50% of saturation) ②	t_{vd}	—	80 (-128Q) –		—	100 (-256Q) –		ns
		—	120 (-256Q) –		—	150 (-512Q) –		ns
		—	160 (-512Q) –		—	200 (-1024Q) –		ns
Clock Pulse Line Capacitance (ϕ1, ϕ2) at 5V bias	Cϕ	—	20 (-128Q) –		—	26 (-256Q) –		pF
		—	37 (-256Q) –		—	50 (-512Q) –		pF
		—	72 (-512Q) –		—	93 (-1024Q) –		pF
Video Line Capacitance at 2V bias	C_V	—	9 (-128Q) –		—	9 (-256Q) –		pF
		—	14 (-256Q) –		—	14 (-512Q) –		pF
		—	27 (-512Q) –		—	27 (-1024Q) –		pF
Power Consumption	P	—	—	1	—	—	1	mW

① V_ϕ is supply clock amplitude.
② Measured with Hamamatsu C4069 driver/amplifier circuit.

ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

Parameters	Symbols	S3901 Series			S3904 Series			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Photodiode Pitch		—	50	—	—	25	—	μm
Photodiode Height		—	2.5	—	—	2.5	—	mm
Photodiode Dark Current ①	I_d	—	0.4	0.6	—	0.2	0.3	pA
Photodiode Capacitance ①	C_{ph}	—	20	—	—	10	—	pF
Spectral Response (20% of peak)	λ	200 to 1000			200 to 1000			nm
Wavelength of Peak Response	λp	—	600	—	—	600	—	nm
Saturation Exposure ①	E_{sat}	—	80	—	—	80	—	mlx•s
Saturation Charge ①	Q_{sat}	—	40	—	—	20	—	pC
Sensitivity Uniformity (50% of saturation, excluding first and last elements)		—	—	±3	—	—	±3	%

① Video bias voltage: 2.0V, Supply clock amplitude: 5.0V

Figure 3: Typical Spectral Response

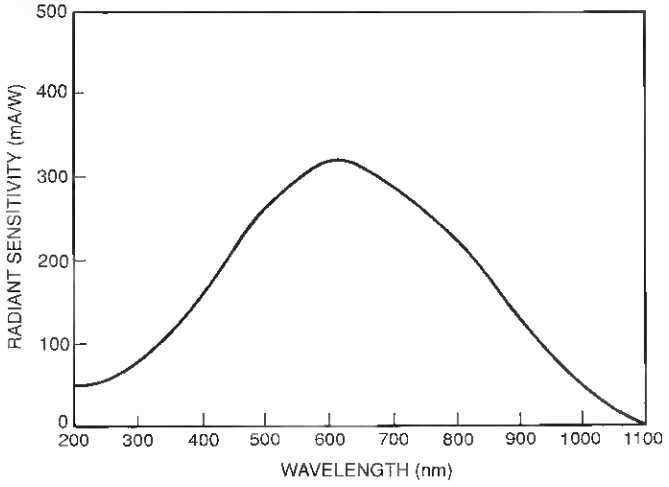
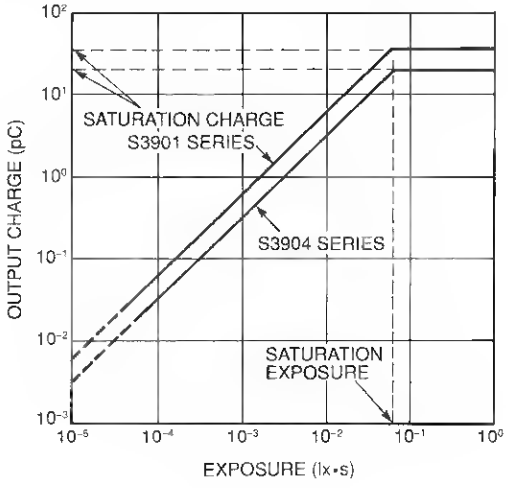
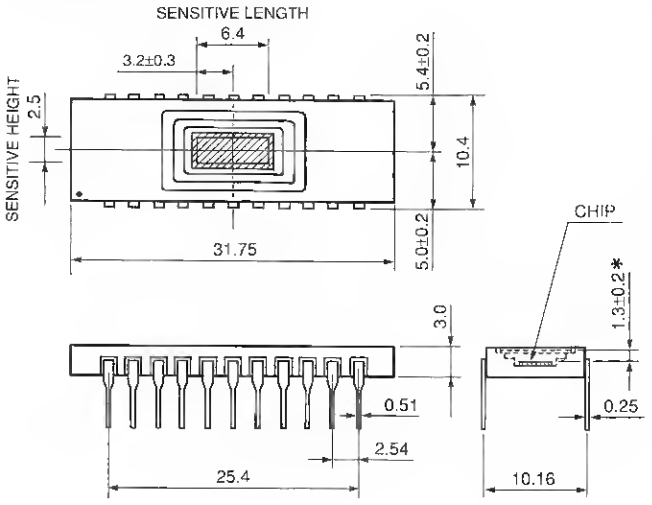


Figure 4: Output Charge vs. Exposure

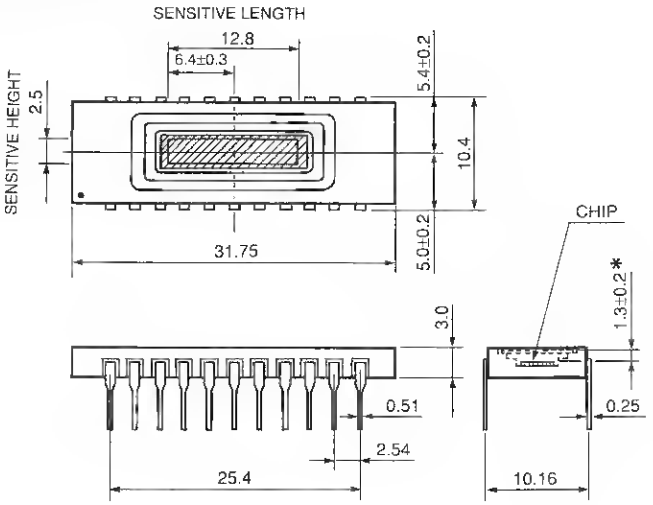


DIMENSIONAL OUTLINES (Unit: mm)

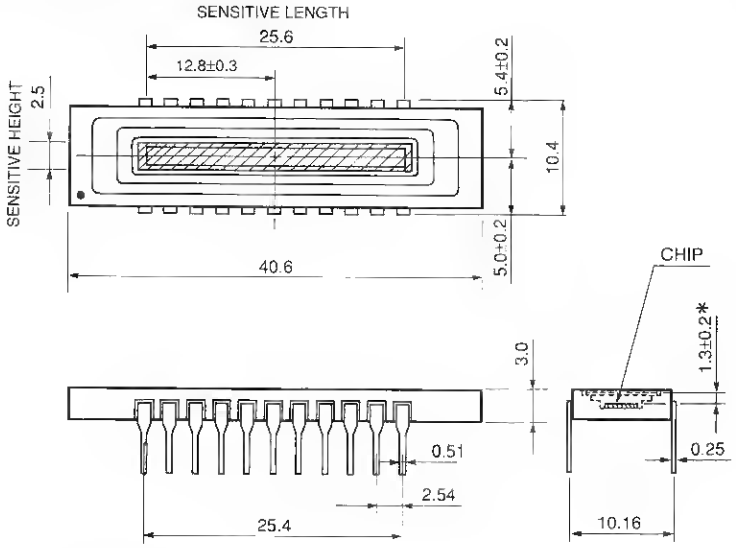
S3901–128Q
S3904–256Q



S3901–256Q
S3904–512Q



S3901–512Q
S3904–1024Q



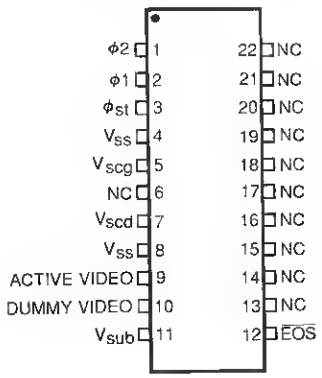
* Optical distance from the outer surface of the quartz window to the chip surface.

• Mechanical Specifications

Parameters	S3901 –128Q	S3901 –256Q	S3901 –512Q	S3904 –256Q	S3904 –512Q	S3904 –1024Q	Units
Number of Photodiodes	128	256	512	256	512	1024	—
Ceramic Length	31.75		40.6	31.75		40.6	mm
Number of Pins	22			22			—
Window Material ①	Quartz			Quartz			—
Net Weight	3.0		3.5	3.0		3.5	g

① Fiber optic window is available

PINOUT AND RECOMMENDED OPERATING CONDITIONS



V_{SS}, V_{sub} and NC should be grounded.

Terminals	Input or Output	Description
$\phi 1$, $\phi 2$	Input (CMOS logic compatible)	Pulses for operating the MOS shift register. As the video output signal is obtained being synchronized with the rise of $\phi 2$, the video data rate is equal to the clock pulse frequency.
ϕ_{st}	Input (CMOS logic compatible)	Pulse for start operating the MOS shift register. The time interval between start pulses is equal to the signal accumulation time.
V_{SS}	Passive node	Connected with the anode of each photodiode. This should be grounded.
V_{scg}	Input	Used for restricting blooming. This shoud be grounded when it is not necessary.
V_{scd}	Input	Used for restricting blooming. This shoud be biased at a voltage equal to the video bias even when it is not necessary.
ACTIVE VIDEO	Output	Video output signal. A positive voltage should be applied to the video line connecting with photodiode cathodes so that each photodiode is reverse-biased. It is recommended that the video bias be 2V when the amplitude of $\phi 1$, $\phi 2$ and ϕ_{st} is at 5V.
DUMMY VIDEO	Output	This has the same structure as the active video, but is not connected with photodiodes, so only spike noise is output. It should be biased at a voltage equal to the active video line. Open circuit when it is not necessary.
V_{sub}	Passive node	Connected with the silicon substrate. This should be grounded.
$\overline{EOS}$	Output (CMOS logic compatible)	This should be pulled up at 5V using a 10kΩ resistor. Negative polarity. This is obtained synchronously with the $\phi 2$ timing right after the last photodiode is addressed.
NC		No connection. These should be grounded.

DRIVER CIRCUIT

• Driver Circuit

No DC supply voltage is required for driving the S3901 and S3904 series MOS linear image sensors. The V_{SS}, V_{sub} and all NC terminals should be grounded, however. Driving the MOS shift register requires a start pulse (ϕst) and two-phase clock pulses (ϕ1, ϕ2). The polarities of ϕst, ϕ1 and ϕ2 are positive and these pulses are CMOS logic compatible.

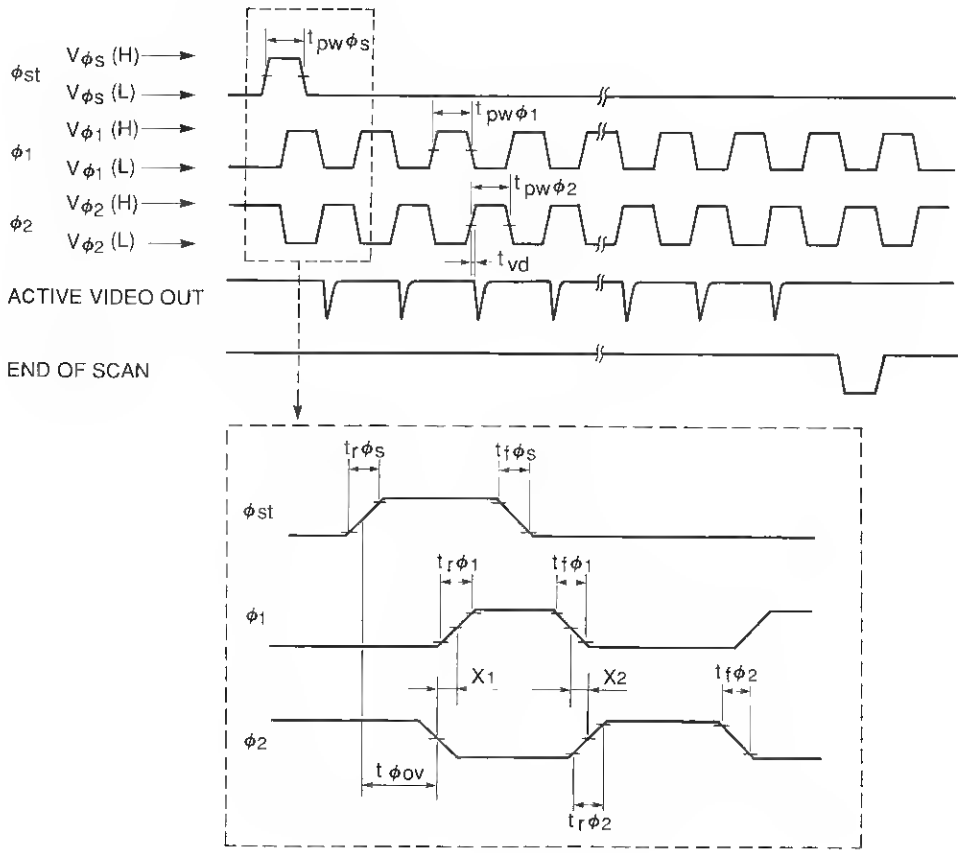
ϕ1 and ϕ2 can be either fully separated or in the complementary relation. However, the overlap should not exceed 50% of the rise or fall edge between ϕ1 and ϕ2, and the pulsewidth of ϕ1 and ϕ2 must be longer than 200 ns. Since the photodiode signal is obtained at the rise of every ϕ2, the clock pulse frequency determines the video data rate.

The amplitude of ϕst should be equal to that of ϕ1 and ϕ2. The shift register starts to read out the signal with the high level of ϕst, so the time interval of each ϕst determines the signal accumulation time. The pulsewidth of ϕst must also be longer than 200ns and must be overlapped with ϕ2 for at least 200ns. Moreover, in order to start the shift register normally, ϕ2 must be changed only once from the high level to the low level during the high level of ϕst. The timing diagram for each pulse is shown in Figure 5.

• End of Scan ($\overline{EOS}$)

By wiring the $\overline{EOS}$ terminal at 5V using a pull-up resistor of 10kΩ, the end of scan signal is obtained, being synchronized with the ϕ2 timing right after the last photodiode is addressed.

Figure 5: Timing Diagram for Drive Circuit



• Signal Readout Circuit

Signal readout methods consist of the current-detection mode (current-voltage conversion mode) using a resistive load and the current-integration mode using a charge amplifier. In either method, a positive bias must be applied to the video line because the photodiode anode of MOS linear image sensors is at 0V (V_{SS}). Figure 6 shows the video bias voltage margin. Higher supply clock amplitude allows larger video bias and saturation charge. Conversely, if the video bias is set at a low level with higher supply clock amplitude, the fall time of video output waveform can be shortend. It is recommended that the video bias be set at 2V when the amplitude of ϕ1, ϕ2 and ϕst is 5V.

To obtain good output linearity, the current-integration mode is suggested. In this mode, immediately before the each photodiode is addressed each time, the integration capacitance is reset at the reference voltage level, and when the address switch is turned on, the signal charge is accumulated in the integration capacitance. Figure 7 shows an example of the current-integration circuit and the pulse timing. To obtain a stable output, the rise edge of the reset pulse should be delayed at least 50 ns from the fall edge of $\phi 2$.

Hamamatsu provides driver/amplifier circuits; the C4070 for the current-integration mode and the C4069 for the current-voltage conversion mode. In addition, the C4091 pulse generator is available, which supplies these driver/amplifier circuits with a master start pulse and master clock pulse.

Figure 6: Video Bias Voltage Margin

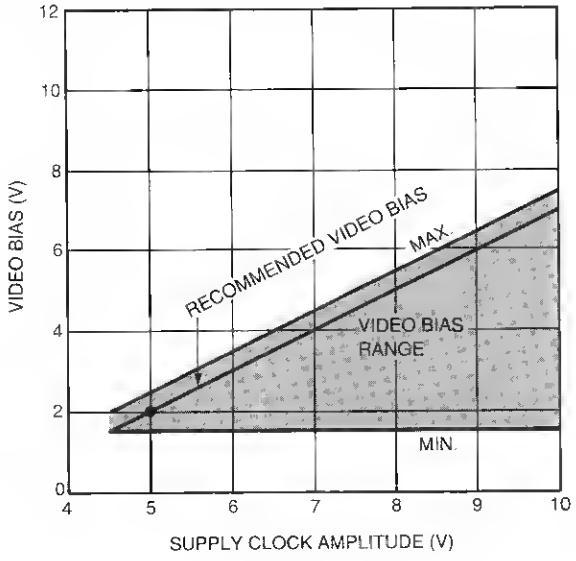
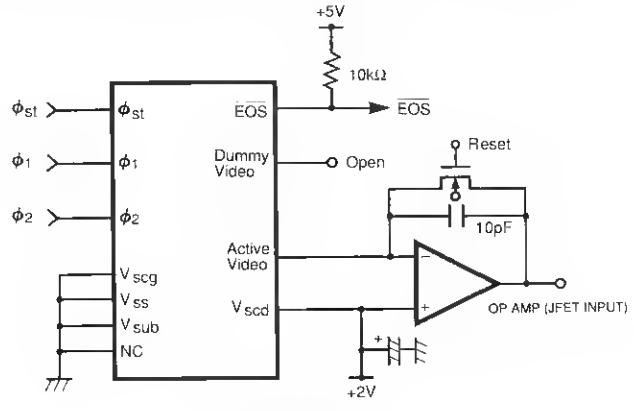
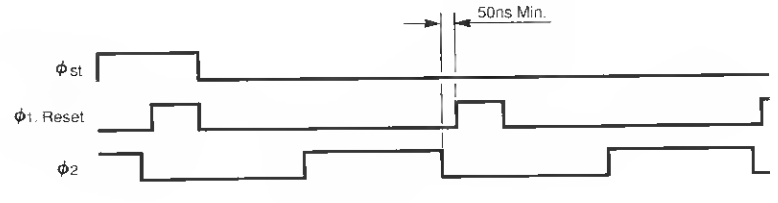


Figure 7: Recommended Readout Circuit and Timing Diagram



READOUT CIRCUIT



PULSE TIMING

• Operation for Saturation Control

When the MOS linear image sensor is used at a light level lower than the saturation exposure, the saturation control function is not necessary. The saturation control drain should be set at a voltage equal to the video bias, and the gate should be grounded.

When light higher than the saturation exposure strikes the sensitive area, even partially, the photodiode cannot accumulate a signal charge exceeding the saturation charge amount. The excessive charge begins to overflow into the video line, thus causing deterioration of the signal purity. In order to eliminate this phenomenon, a voltage equal to the video bias (typically 2V) should be given to the saturation control drain. Also, a bias voltage should be applied to the saturation control gate so that the saturation charge amount is set at the desired level. The larger the bias voltage for the saturation control gate, the higher the saturation control function will be. However, a larger bias voltage also causes a decrease in the saturation charge amount. Therefore, it is necessary to select the appropriate bias voltage value carefully.

APPENDIX

1) **Operation for all photodiode reset:**
In normal operation, the charge accumulated in the photodiode is reset when the signal is read out. For the S3901 and S3904 series, the signal charge can be reset at a line other than the signal readout. This is done by adding an appropriate pulse to the saturation control gate. The amplitude of this pulse should be equal to $\phi 1$, $\phi 2$ and ϕst, and the pulsewidth should be longer than 5μs.

When the saturation control gate is set at the high level, all photodiodes are reset simultaneously at the potential of the saturation control drain. (This is set at the same potential as the video bias, and is typically 2V.) On the contrary, when the saturation control gate is set at the low level, the signal charge accumulates in the photodiode without a reset being carried out.

2) **Dummy video:**
The S3901 and S3904 series have a dummy video line to eliminate spike noise in the video output waveform. Video signal with lower spike noise can be obtained by the differential amplification between the active video line and dummy video line outputs. But, in normal operation, the dummy video line need not to be used. Leave it unconnected.

HAMAMATSU

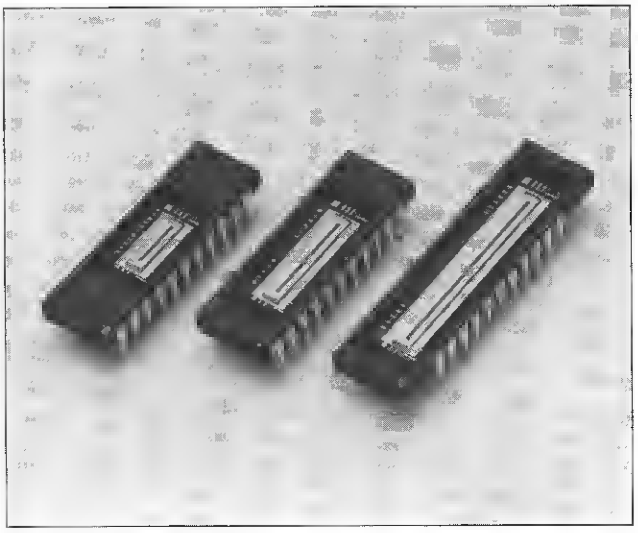
TECHNICAL DATA

SERIAL/CURRENT OUTPUT TYPE MOS LINEAR IMAGE SENSORS S3902, S3903 SERIES

High UV Sensitivity, 0.5mm Photodiode Height, Excellent Photometric Capabilities, Low Power Consumption

FEATURES

- **Medium wide photosensitive area**
  Photodiode pitch : 50μm (S3902), 25μm (S3903)
  Photodiode height : 0.5mm
- **High UV sensitivity with good stability**
- **Excellent photometric capabilities**
  Low dark current and high saturation charge
  Good linearity
  Wide dynamic range
- **Low power consumption : less than 1mW**
- **Start pulse and clock pulses are CMOS logic compatible**



APPLICATIONS

- **Multichannel spectrophotometry**
- **Image readout systems**

DESCRIPTION

By applying NMOS technology to the manufacture of self-scanning linear photodiode arrays, Hamamatsu can offer higher performance and increased flexibility to photometric instrument manufacturers. The new design achieves high UV sensitivity without deterioration even by extended UV exposure. Application is simplified because of low power consumption and single video output line. All members of the series are pin compatible.

The S3902 and S3903 series MOS linear image sensors feature a good linearity over a wide dynamic range and low power consumption, and a photosensitive area of 0.5mm photodiode height with a photodiode pitch of 50μm (S3902) or 25μm (S3903). Each series is available with three different number of photodiodes; 128, 256 and 512 for the S3902 series, 256, 512 and 1024 for the S3903 series.

Figure 1: Equivalent Circuit

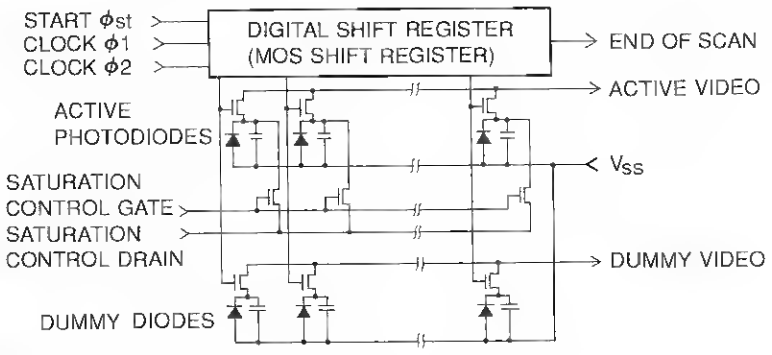
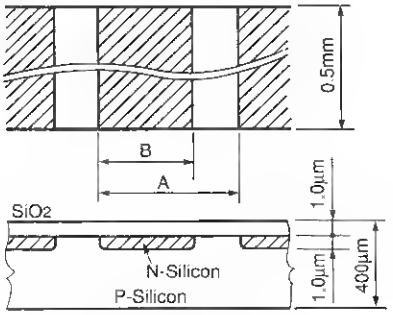


Figure 2: Sensor Geometry



S3902: A=50μm, B=45μm
S3903: A=25μm, B=20μm

MAXIMUM RATINGS

Parameters	Symbols	S3902, S3903 Series	Units
Supply Clock Amplitude	$V\phi$	15	V
Qperating Temperature ①	Topr	−40 to +65	°C
Storage Temperature	Tstg	−40 to +85	°C

① No dew

ELECTRICAL CHARACTERISTICS (Ta=25°C)

Parameters	Symbols	S3902 Series			S3903 Series			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Video Bias Voltage ①	V_b	1.5	$V\phi$−3.0	$V\phi$−2.5	1.5	$V\phi$−3.0	$V\phi$−2.5	V
Saturation Control Gate Voltage	V_{scg}	—	0	—	—	0	—	V
Saturation Control Drain Voltage	V_{scd}	—	V_b	—	—	V_b	—	V
Start Pulse Voltage (ϕst) ① -High	$V_{\phi s}$(H)	4.5	$V\phi$	10	4.5	$V\phi$	10	V
-Low	$V_{\phi s}$(L)	0	—	0.4	0	—	0.4	V
Clock Pulse Voltage (ϕ1, ϕ2) -High	Vϕ1, Vϕ2(H)	4.5	5	10	4.5	5	10	V
-Low	Vϕ1, Vϕ2(L)	0	—	0.4	0	—	0.4	V
Start Pulse Rise/Fall Times (ϕst)	$t_{r\phi s}$, $t_{f\phi s}$	—	—	500	—	—	500	ns
Start Pulsewidth (ϕst)	$t_{pw\phi s}$	200	—	—	200	—	—	ns
Clock Pulse Rise/Fall Times (ϕ1, ϕ2)	$t_{r\phi 1}$, $t_{r\phi 2}$, $t_{f\phi 1}$, $t_{f\phi 2}$	—	—	500	—	—	500	ns
Clock Pulsewidth (ϕ1, ϕ2)	$t_{pw\phi 1}$, $t_{pw\phi 2}$	200	—	—	200	—	—	ns
Start Pulse (ϕst) and Clock Pulse (ϕ2) Overlap	$t_{\phi ov}$	200	—	—	200	—	—	ns
Clock Pulse Space	X_1, X_2	0	—	—	0	—	—	ns
Data Rate	f	0.1	—	2000	0.1	—	2000	kHz
Video Delay Time (50% of saturation) ②	t_{vd}	—	70 (-128Q) –		—	80 (-256Q) –		ns
		—	110 (-256Q) –		—	120 (-512Q) –		ns
		—	140 (-512Q) –		—	160 (-1024Q) –		ns
Clock Pulse Line Capacitance (ϕ1, ϕ2) at 5V bias	$C\phi$	—	20 (-128Q) –		—	26 (-256Q) –		pF
		—	37 (-256Q) –		—	50 (-512Q) –		pF
		—	72 (-512Q) –		—	93 (-1024Q) –		pF
Video Line Capacitance at 2V bias	C_V	—	9 (-128Q) –		—	9 (-256Q) –		pF
		—	14 (-256Q) –		—	14 (-512Q) –		pF
		—	27 (-512Q) –		—	27 (-1024Q) –		pF
Power Consumption	P	—	—	1	—	—	1	mW

① $V\phi$ is supply clock amplitude.
② Measured with Hamamatsu C4069 driver/amplifier circuit.

ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

Parameters	Symbols	S3902 Series			S3903 Series			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Photodiode Pitch		—	50	—	—	25	—	μm
Photodiode Height		—	0.5	—	—	0.5	—	mm
Photodiode Dark Current ①	I_d	—	0.1	0.15	—	0.05	0.08	pA
Photodiode Capacitance ①	C_{ph}	—	4	—	—	2	—	pF
Spectral Response (20% of peak)	λ	200 to 1000			200 to 1000			nm
Wavelength of Peak Response	λp	—	600	—	—	600	—	nm
Saturation Exposure ①	E_{sat}	—	80	—	—	80	—	mlx•s
Saturation Charge ①	Q_{sat}	—	8	—	—	4	—	pC
Sensitivity Uniformity (50% of saturation, excluding first and last elements)		—	—	±3	—	—	±3	%

① Video bias voltage: 2.0V, Supply clock amplitude: 5.0V

Figure 3: Typical Spectral Response

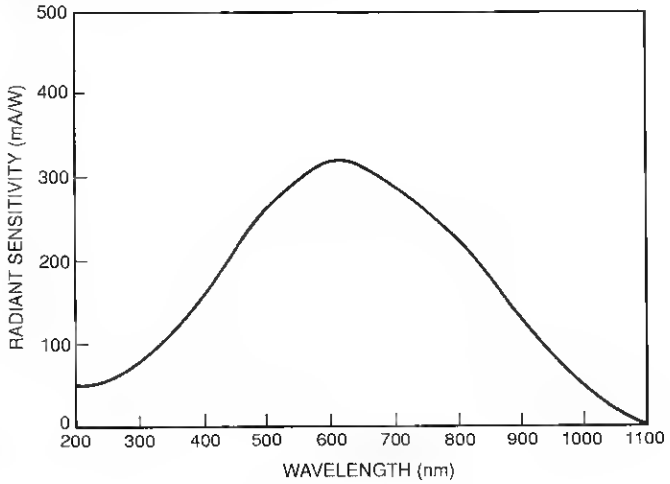
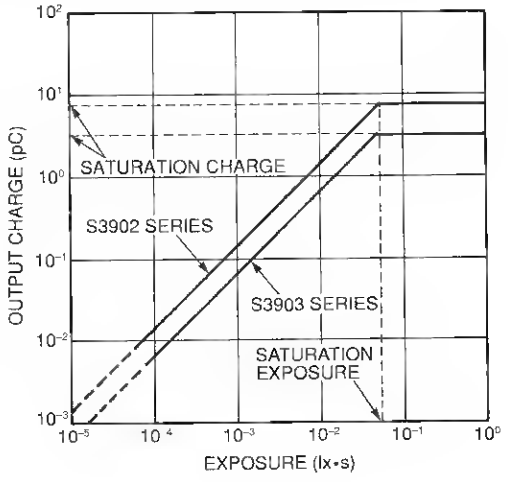
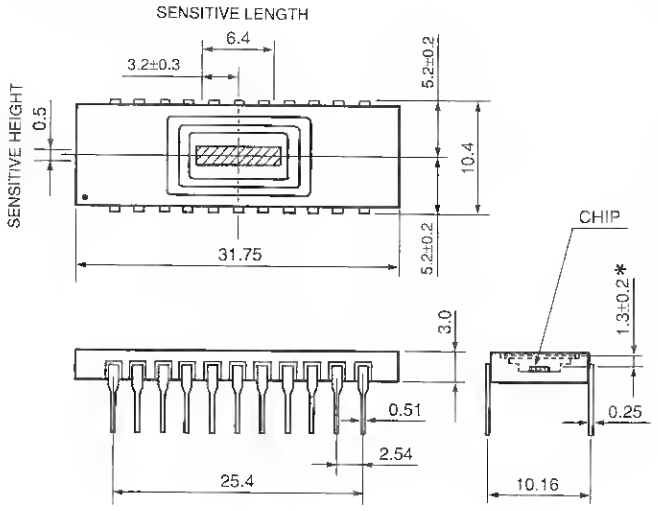


Figure 4: Output Charge vs. Exposure

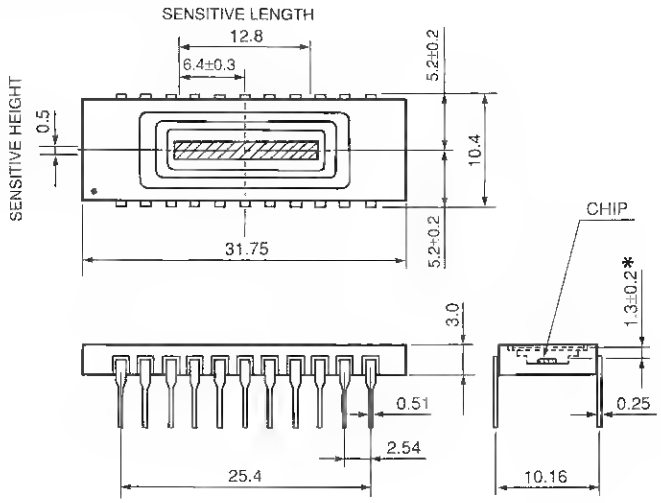


DIMENSIONAL OUTLINES (Unit: mm)

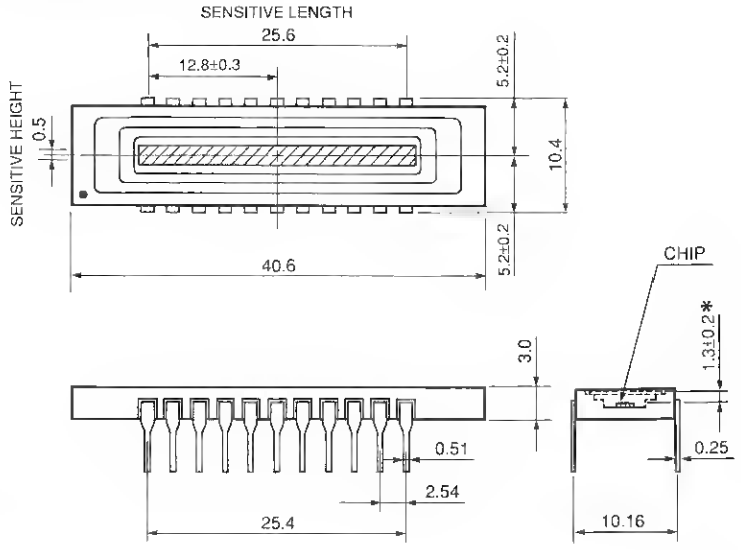
S3902–128Q
S3903–256Q



S3902–256Q
S3903–512Q



S3902–512Q
S3903–1024Q



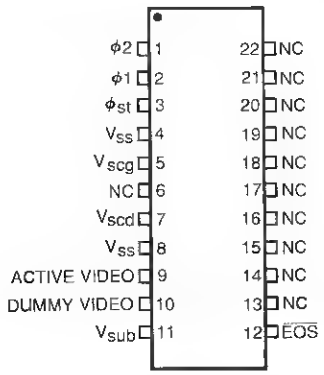
* Optical distance from the outer surface of the quartz window to the chip surface.

• Mechanical Specifications

Parameters	S3902 –128Q	S3902 –256Q	S3902 –512Q	S3903 –256Q	S3903 –512Q	S3903 –1024Q	Units
Number of Photodiodes	128	256	512	256	512	1024	—
Ceramic Length	31.75		40.6	31.75		40.6	mm
Number of Pins	22			22			—
Window Material ①	Quartz			Quartz			—
Net Weight	3.0		3.5	3.0		3.5	g

① Fiber optic window is available

PINOUT AND RECOMMENDED OPERATING CONDITIONS



V_{SS}, V_{sub} and NC should be grounded.

Terminals	Input or Output	Description
ϕ1, ϕ2	Input (CMOS logic compatible)	Pulses for operating the MOS shift register. As the video output signal is obtained being synchronized with the rise of ϕ2, the video data rate is equal to the clock pulse frequency.
ϕst	Input (CMOS logic compatible)	Pulse for start operating the MOS shift register. The time interval between start pulses is equal to the signal accumulation time.
V_{SS}	Passive node	Connected with the anode of each photodiode. This should be grounded.
V_{scg}	Input	Used for restricting blooming. This shoud be grounded when it is not necessary.
V_{scd}	Input	Used for restricting blooming. This shoud be biased at a voltage equal to the video bias even when it is not necessary.
ACTIVE VIDEO	Output	Video output signal. A positive voltage should be applied to the video line connecting with photodiode cathodes so that each photodiode is reverse-biased. It is recommended that the video bias be 2V when the amplitude of ϕ1, ϕ2 and ϕ_{st} is at 5V.
DUMMY VIDEO	Output	This has the same structure as the active video, but is not connected with photodiodes, so only spike noise is output. It should be biased at a voltage equal to the active video line. Open circuit when it is not necessary.
V_{sub}	Passive node	Connected with the silicon substrate. This should be grounded.
$\overline{EOS}$	Output (CMOS logic compatible)	This should be pulled up at 5V using a 10kΩ resistor. Negative polarity. This is obtained synchronously with the ϕ2 timing right after the last photodiode is addressed.
NC		No connection. These should be grounded.

DRIVER CIRCUIT

• Driver Circuit

No DC supply voltage is required for driving the S3902 and S3903 series MOS linear image sensors. The V_{SS}, V_{sub} and all NC terminals should be grounded, however. Driving the MOS shift register requires a start pulse (ϕst) and two-phase clock pulses (ϕ1, ϕ2). The polarities of ϕst, ϕ1 and ϕ2 are positive and these pulses are CMOS logic compatible.

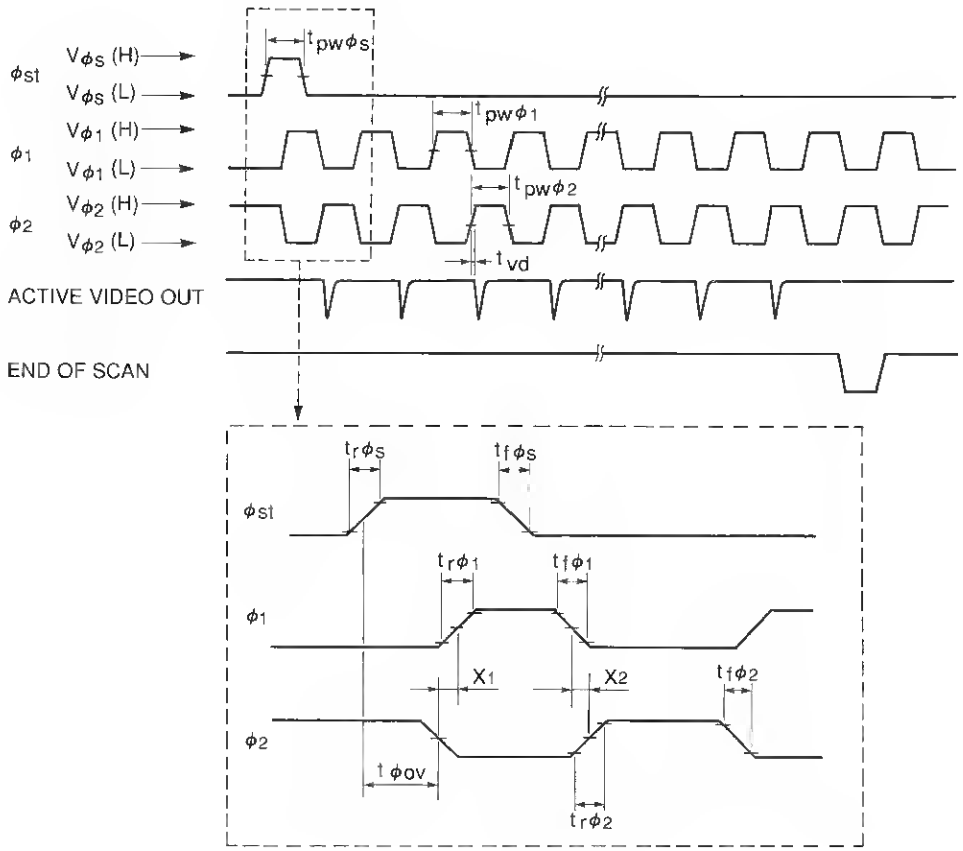
ϕ1 and ϕ2 can be either fully separated or in the complementary relation. However, the overlap should not exceed 50% of the rise or fall edge between ϕ1 and ϕ2, and the pulsewidth of ϕ1 and ϕ2 must be longer than 200 ns. Since the photodiode signal is obtained at the rise of every ϕ2, the clock pulse frequency determines the video data rate.

The amplitude of ϕst should be equal to that of ϕ1 and ϕ2. The shift register starts to read out the signal with the high level of ϕst, so the time interval of each ϕst determines the signal accumulation time. The pulsewidth of ϕst must also be longer than 200ns and must be overlapped with ϕ2 for at least 200ns. Moreover, in order to start the shift register normally, ϕ2 must be changed only once from the high level to the low level during the high level of ϕst. The timing diagram for each pulse is shown in Figure 5.

• End of Scan ($\overline{EOS}$)

By wiring the $\overline{EOS}$ terminal at 5V using a pull-up resistor of 10kΩ, the end of scan signal is obtained, being synchronized with the ϕ2 timing right after the last photodiode is addressed.

Figure 5: Timing Diagram for Drive Circuit



• Signal Readout Circuit

Signal readout methods consist of the current-detection mode (current-voltage conversion mode) using a resistive load and the current-integration mode using a charge amplifier. In either method, a positive bias must be applied to the video line because the photodiode anode of MOS linear image sensors is at 0V (V_{SS}). Figure 6 shows the video bias voltage margin. Higher supply clock amplitude allows larger video bias and saturation charge. Conversely, if the video bias is set at a low level with higher supply clock amplitude, the fall time of video output waveform can be shortend. It is recommended that the video bias be set at 2V when the amplitude of ϕ1, ϕ2 and ϕst is 5V.

To obtain good output linearity, the current-integration mode is suggested. In this mode, immediately before the each photodiode is addressed each time, the integration capacitance is reset at the reference voltage level, and when the address switch is turned on, the signal charge is accumulated in the integration capacitance. Figure 7 shows an example of the current-integration circuit and the pulse timing. To obtain a stable output, the rise edge of the reset pulse should be delayed at least 50 ns from the fall edge of $\phi 2$.

Hamamatsu provides driver/amplifier circuits; the C4070 for the current-integration mode and the C4069 for the current-voltage conversion mode. In addition, the C4091 pulse generator is available, which supplies these driver/amplifier circuits with a master start pulse and master clock pulse.

Figure 6: Video Bias Voltage Margin

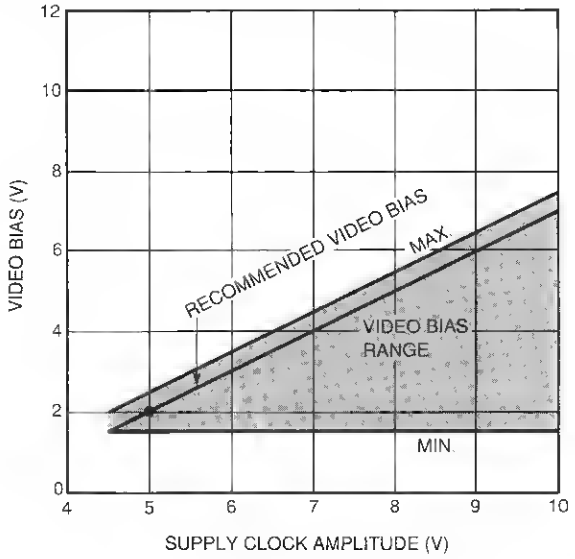
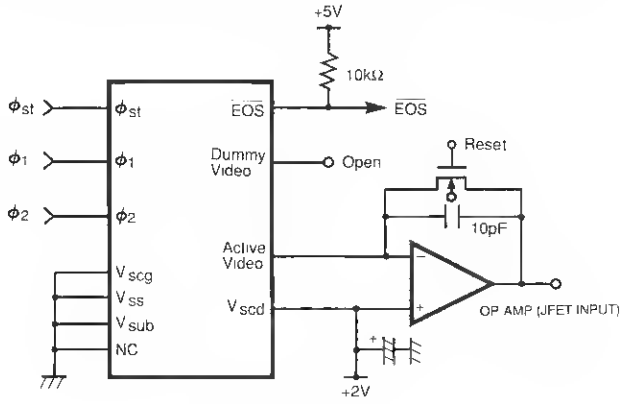
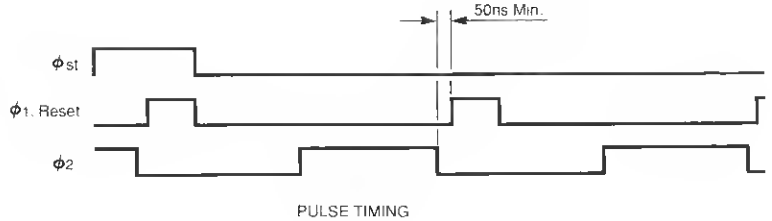


Figure 7: Recommended Readout Circuit and Timing Diagram



READOUT CIRCUIT



PULSE TIMING

• Operation for Saturation Control

When the MOS linear image sensor is used at a light level lower than the saturation exposure, the saturation control function is not necessary. The saturation control drain should be set at a voltage equal to the video bias, and the gate should be grounded.

When light higher than the saturation exposure strikes the sensitive area, even partially, the photodiode cannot accumulate a signal charge exceeding the saturation charge amount. The excessive charge begins to overflow into the video line, thus causing deterioration of the signal purity. In order to eliminate this phenomenon, a voltage equal to the video bias (typically 2V) should be given to the saturation control drain. Also, a bias voltage should be applied to the saturation control gate so that the saturation charge amount is set at the desired level. The larger the bias voltage for the saturation control gate, the higher the saturation control function will be. However, a larger bias voltage also causes a decrease in the saturation charge amount. Therefore, it is necessary to select the appropriate bias voltage value carefully.

APPENDIX

1) **Operation for all photodiode reset:**
In normal operation, the charge accumulated in the photodiode is reset when the signal is read out. For the S3902 and S3903 series, the signal charge can be reset at a line other than the signal readout. This is done by adding an appropriate pulse to the saturation control gate. The amplitude of this pulse should be equal to $\phi 1$, $\phi 2$ and ϕst, and the pulsewidth should be longer than 5μs.

When the saturation control gate is set at the high level, all photodiodes are reset simultaneously at the potential of the saturation control drain. (This is set at the same potential as the video bias, and is typically 2V.) On the contrary, when the saturation control gate is set at the low level, the signal charge accumulates in the photodiode without a reset being carried out.

2) **Dummy video:**
The S3902 and S3903 series have a dummy video line to eliminate spike noise in the video output waveform. Video signal with lower spike noise can be obtained by the differential amplification between the active video line and dummy video line outputs. But, in normal operation, the dummy video line need not to be used. Leave it unconnected.

HAMAMATSU

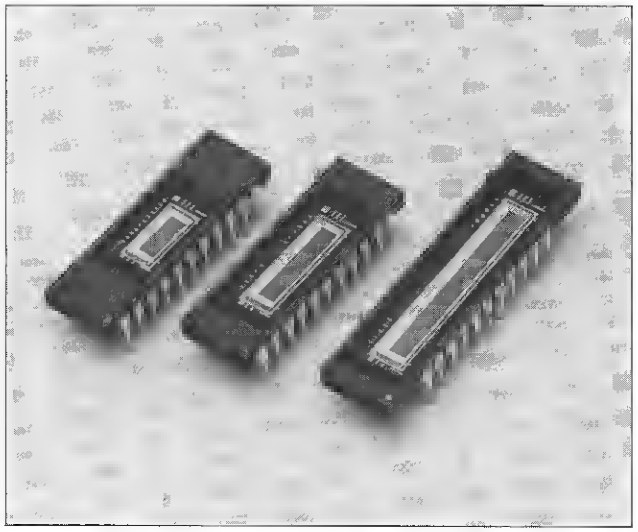
TECHNICAL DATA

SERIAL/VOLTAGE OUTPUT TYPE MOS LINEAR IMAGE SENSORS S3921, S3924 SERIES

Wide Sensitive Area (2.5mm Photodiode Height), High UV Sensitivity, Integrated Signal Processing Circuit Provides Boxcar Output Waveform

FEATURES

- **Integrated signal processing circuit provides boxcar output waveform for simple readout**
- **Wide photosensitive area**
  Photodiode pitch : 50μm (S3921), 25μm (S3924)
  Photodiode height : 2.5mm
- **High UV sensitivity with good stability**
- **Excellent photometric capabilities**
  Low dark current and high saturation charge
  Wide dynamic range
- **Operatable with low voltage, single power supply**
- **Low power consumption**
- **Start pulse, clock pulses and video-line reset pulse are CMOS logic compatible**



APPLICATIONS

- **Multichannel spectrophotometry**
- **Image readout systems**

DESCRIPTION

By applying NMOS technology to the manufacture of self-scanning linear photodiode arrays, Hamamatsu can offer higher performance and increased flexibility to photometric instrument manufacturers. The new design achieves high UV sensitivity without deterioration even by extended UV exposure. Application is simplified because of single supply operation, low power consumption, and single video output line. All members of the series are pin compatible.

The S3921 and S3924 MOS linear image sensors feature a signal processing circuit which integrates a signal charge in the video line and performs impedance conversion to provide output signal with boxcar waveform. This allows signal readout with a simple external circuit. The S3921 and S3924 also have a wide photosensitive area of 2.5mm photodiode height and 50μm (S3921) or 25μm (S3924) photodiode pitch.

Figure 1: Equivalent Circuit

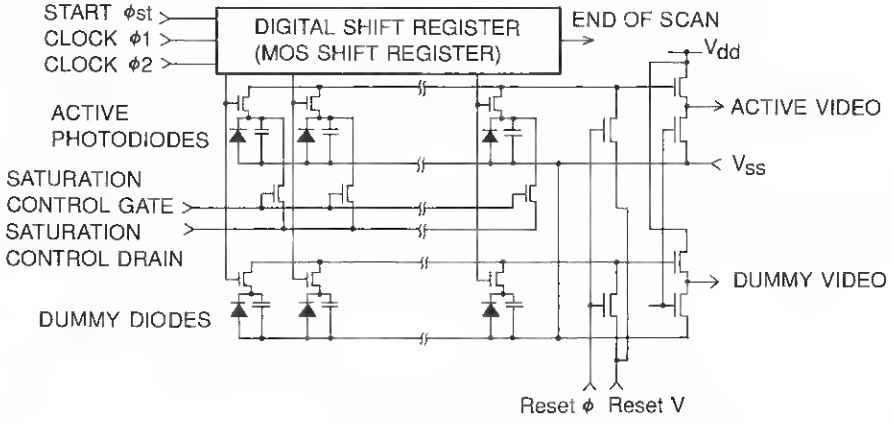
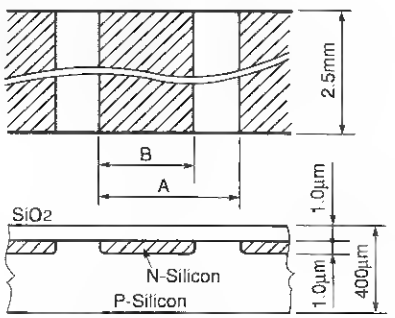


Figure 2: Sensor Geometry



S3921: A=50μm, B=45μm
S3924: A=25μm, B=20μm

MAXIMUM RATINGS

Parameters	Symbols	S3921, S3924	Units
Supply Voltage	V_{dd}	15	V
Supply Clock Amplitude	$V\phi$	15	V
Operating Temperature ①	Topr	−40 to +65	°C
Storage Temperature	Tstg	−40 to +85	°C

① No dew

ELECTRICAL CHARACTERISTICS (Ta=25°C)

Parameters	Symbols	S3921 Series			S3924 Series			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage for Source Follower Circuit ①	V_{dd}	4.5	$V\phi$	10	4.5	$V\phi$	10	V
Reset Voltage (Reset V) ②	V_r	2.0	$V\phi$−2.5	$V\phi$−2.0	2.0	$V\phi$−2.5	$V\phi$−2.0	V
Saturation Control Gate Voltage	V_{scg}	—	0	—	—	0	—	V
Saturation Control Drain Voltage ②	V_{scd}	—	V_r	—	—	V_r	—	V
Start Pulse Voltage (ϕst) ① -High	$V_{\phi s}$(H)	4.5	$V\phi$	10	4.5	$V\phi$	10	V
-Low	$V_{\phi s}$(L)	0	—	0.4	0	—	0.4	V
Clock Pulse Voltage (ϕ1, ϕ2) -High	$V\phi$1, $V\phi$2(H)	4.5	5	10	4.5	5	10	V
-Low	$V\phi$1, $V\phi$2(L)	0	—	0.4	0	—	0.4	V
Reset Pulse Voltage (Reset ϕ) ① -High	$V_{r\phi}$(H)	4.5	$V\phi$	10	4.5	$V\phi$	10	V
-Low	$V_{r\phi}$(L)	0	—	0.4	0	—	0.4	V
Start Pulse Rise/Fall Times (ϕst)	$t_{r\phi s}$, $t_{f\phi s}$	—	—	500	—	—	500	ns
Start Pulsewidth (ϕst)	$t_{pw\phi s}$	200	—	—	200	—	—	ns
Clock Pulse Rise/Fall Times (ϕ1, ϕ2)	$t_{r\phi1}$, $t_{r\phi2}$, $t_{f\phi1}$, $t_{f\phi2}$	—	—	500	—	—	500	ns
Clock Pulsewidth (ϕ1, ϕ2)	$t_{pw\phi1}$, $t_{pw\phi2}$	200	—	—	200	—	—	ns
Reset Pulse Rise/Fall Times	$t_{rr\phi}$, $t_{fr\phi}$	—	—	500	—	—	500	ns
Start Pulse (ϕst) and Clock Pulse (ϕ2) Qverlap	$t_{\phi ov}$	200	—	—	200	—	—	ns
Clock Pulse (ϕ2) and Reset Pulse (Reset ϕ) Qverlap	$t_{\phi ovr}$	660	—	—	660	—	—	ns
Clock Pulse (ϕ2) to Reset Pulse (Reset ϕ) Delay Time	$t_{d\phi r\text{-}2}$	50	—	—	50	—	—	ns
Clock Pulse Space (ϕ1, ϕ2)	X1, X2	0	—	—	0	—	—	ns
Clock Pulse Space (ϕ2, Reset ϕ)	$t_{s\phi r\text{-}2}$	0	—	—	0	—	—	ns
Data Rate	f	0.1	—	500	0.1	—	500	kHz
Video Delay Time (50% of saturation)	t_{vd}	—	100 (-128Q) –		—	100 (-256Q) –		ns
		—	150 (-256Q) –		—	150 (-512Q) –		ns
		—	200 (-512Q) –		—	200 (-1024Q) –		ns
Clock Pulse Line Capacitance (ϕ1, ϕ2) at 5V bias	$C\phi$	—	20 (-128Q) –		—	26 (-256Q) –		pF
		—	37 (-256Q) –		—	50 (-512Q) –		pF
		—	72 (-512Q) –		—	93 (-1024Q) –		pF
Reset Pulse Line Capacitance (Reset ϕ) at 5V bias	C_r	—	6	—	—	6	—	pF
Qutput Impedance at V_{dd}=5V, V_r=2.5V	Zo	—	200	—	—	200	—	Ω
Power Consumption at V_{dd}=5V, V_r=2.5V	P	—	—	10	—	—	10	mW

① $V\phi$ is supply clock amplitude
② Reset V and saturation control drain use pin 7 in common.

ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

Parameters	Symbols	S3921 Series			S3924 Series			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Photodiode Pitch		—	50	—	—	25	—	μm
Photodiode Height		—	2.5	—	—	2.5	—	mm
Photodiode Dark Current ①	I_d	—	0.4	0.6	—	0.2	0.3	pA
Photodiode Capacitance ①	C_{ph}	—	18	—	—	9	—	pF
Spectral Response (20% of peak)	λ	200 to 1000			200 to 1000			nm
Wavelength of Peak Response	λp	—	600	—	—	600	—	nm
Saturation Exposure ①	E_{sat}	—	55	(-128Q) –	—	70	(-256Q) –	mlx•s
		—	60	(-256Q) –	—	80	(-512Q) –	
		—	80	(-512Q) –	—	80	(-1024Q) –	
Saturation Charge ①	Q_{sat}	—	45	—	—	22.5	—	pC
Saturation Qutput Voltage ①	V_{sat}	—	1000	(-128Q) –	—	1000	(-256Q) –	mV
		—	1000	(-256Q) –	—	810	(-512Q) –	mV
		—	1000	(-512Q) –	—	610	(-1024Q) –	mV
Sensitivity Uniformity (50% of saturation, excluding first and last elements)		—	—	±3	—	—	±3	%

① Reset voltage : 2.5V, V_{dd} : 5V, Supply clock amplitude : 5V

Figure 3: Typical Spectral Response

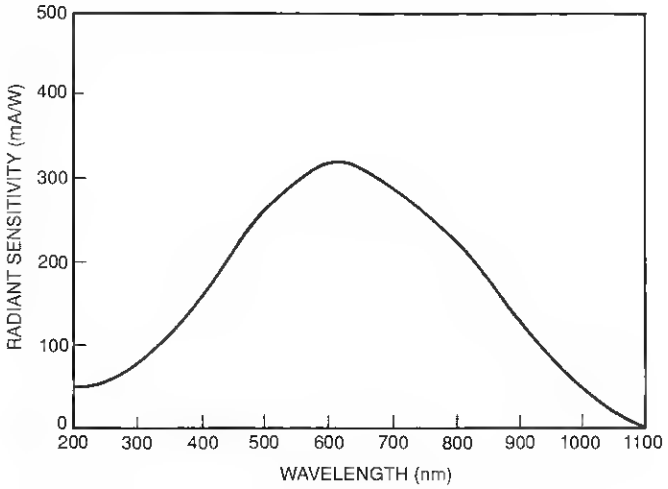
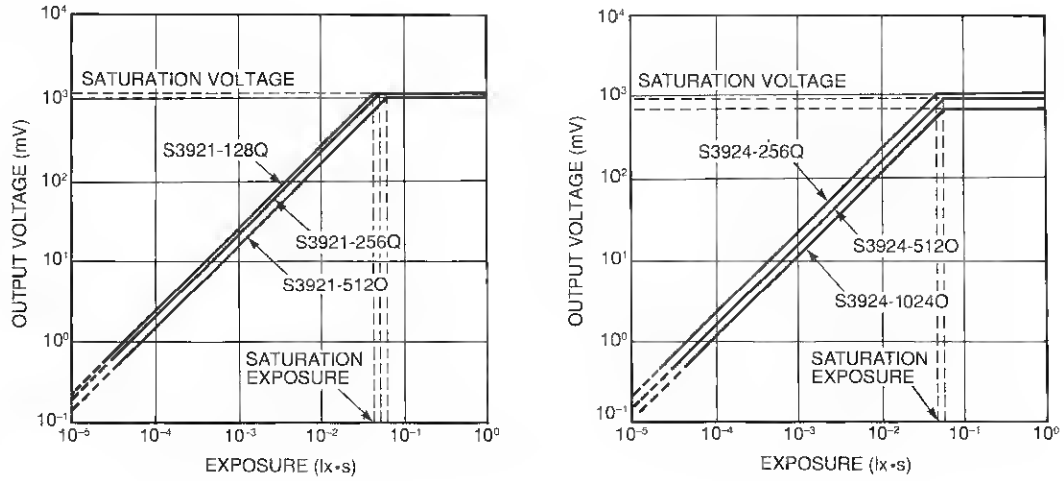
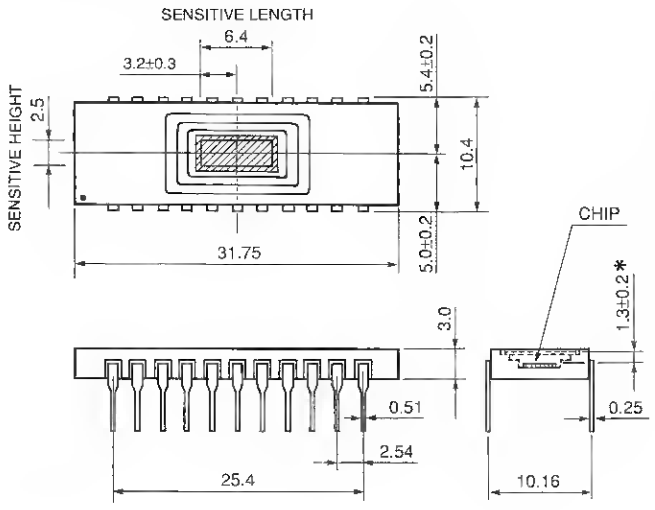


Figure 4: Output Voltage vs. Exposure

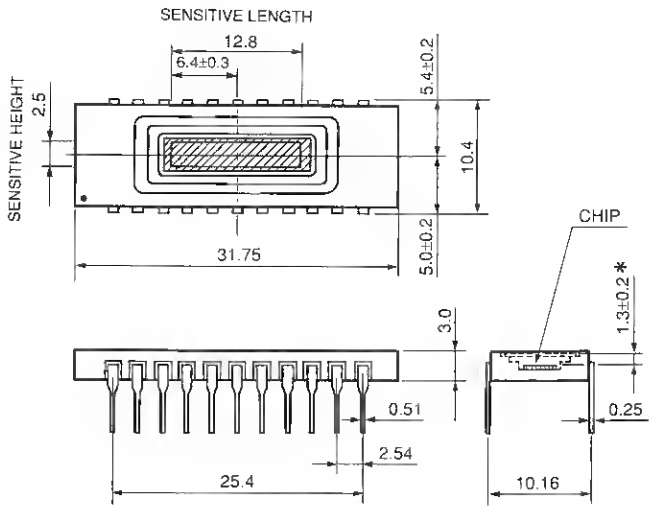


DIMENSIONAL OUTLINES (Unit: mm)

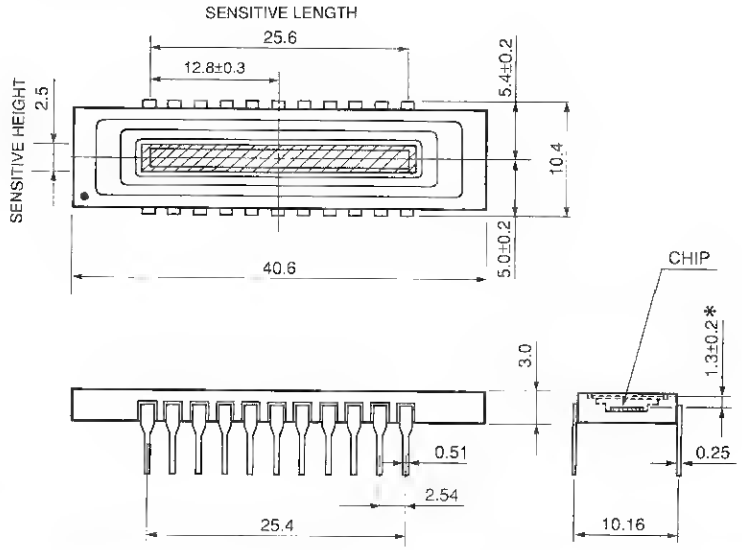
S3921–128Q
S3924–256Q



S3921–256Q
S3924–512Q



S3921–512Q
S3924–1024Q



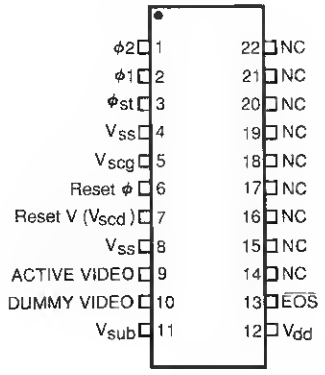
* Optical distance from the outer surface of the quartz window to the chip surface.

• Mechanical Specifications

Parameters	S3921 –128Q	S3921 –256Q	S3921 –512Q	S3924 –256Q	S3924 –512Q	S3924 –1024Q	Units
Number of Photodiodes	128	256	512	256	512	1024	—
Ceramic Length	31.75		40.6	31.75		40.6	mm
Number of Pins	22			22			—
Window Material ①	Quartz			Quartz			—
Net Weight	3.0		3.5	3.0		3.5	g

① Fiber optic window is available.

PINOUT AND RECOMMENDED OPERATING CONDITIONS



V_{SS}, V_{sub} and NC should be grounded.

Terminals	Input or Output	Description
$\phi 1$, $\phi 2$	Input (CMOS logic compatible)	Pulses for operating the MOS shift register. As the video output signal is obtained being synchronized with the rise of $\phi 2$, the video data rate is equal to the clock pulse frequency.
ϕ_{st}	Input (CMOS logic compatible)	Pulse for start operating the MOS shift register. The time interval between start pulses is equal to the signal accumulation time.
V_{ss}	Passive node	Connected with the anode of each photodiode. This should be grounded.
V_{scg}	Input	Used for restricting blooming. This shoud be grounded when it is not necessary.
Reset ϕ	Input (CMOS logic compatible input)	With the high level, the video line is reset at Reset V voltage.
Reset V	Input	A positive voltage should be applied to the video line connecting with photodiode cathodes so that each photodiode is reverse-biased. It is recommended that Reset V be 2.5V when the amplitude of $\phi 1$, $\phi 2$, ϕ_{st} and Reset ϕ is 5V. Reset V and Vscd use pin 7 in common.
V_{scd}	Input	Used for restricting blooming. This should be biased at a voltage equal to Reset V even when it is not necessary.
ACTIVE VIDEO	Output	Low-impedance video output signal after internal current-voltage conversion. Negative polarity output including a DC offset.
DUMMY VIDEO	Output	This has the same structure as the active video, but is not connected with photodiodes, so only DC offset is output. Open circuit when it is not necessary.
V_{sub}	Passive node	Connected with the silicon substrate. This should be grounded.
V_{dd}	Input	Supply voltage to the internal impedance conversion circuit. It should be biased at a voltage equal to the amplitude of each clock (typically 5V).
$\overline{EOS}$	Output (CMOS logic compatible)	This should be pulled up at 5V using a 10kΩ resistor. Negative polarity. This is obtained synchronously with the $\phi 2$ timing right after the last photodiode is addressed.
NC		No connection. These should be grounded.

DRIVER CIRCUIT

• Driver Circuit

Driving the MOS shift register requires a start pulse (ϕst) and two-phase clock pulses (ϕ1, ϕ2). The polarities of ϕst, ϕ1 and ϕ2 are positive and these pulses are CMOS logic compatible.

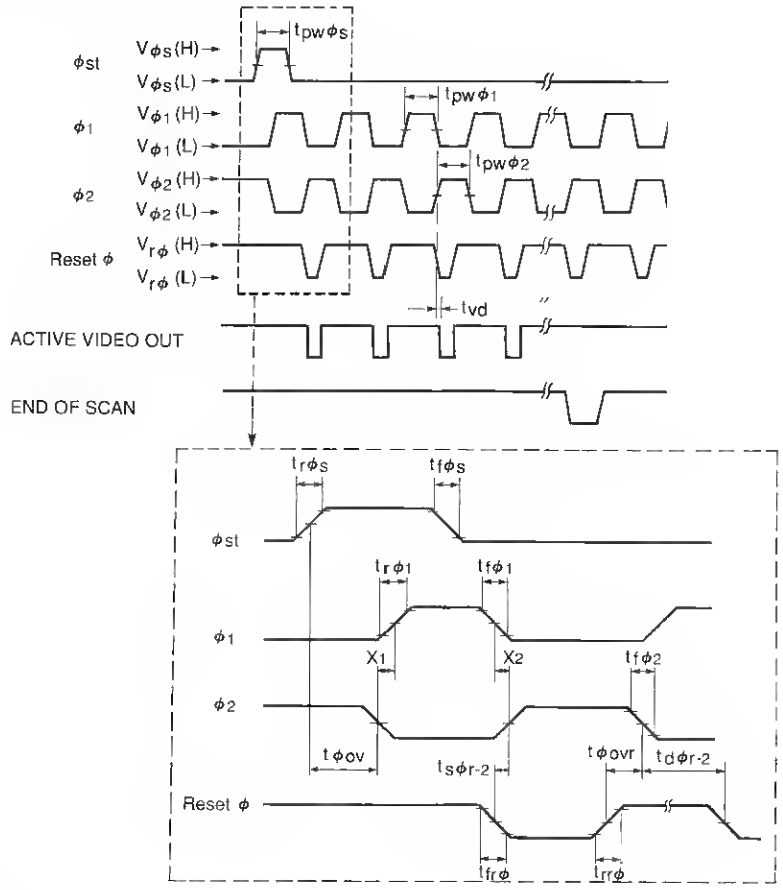
ϕ1 and ϕ2 can be either fully separated or in the complementary relation. However, the overlap should not exceed 50% of the rise or fall edge between ϕ1 and ϕ2. The pulsewidth of ϕ1 and ϕ2 must be longer than 200 ns. Since the photodiode signal is obtained at the rise of every ϕ2, the clock pulse frequency determines the video data rate.

The amplitude of ϕst should be equal to that of ϕ1 and ϕ2. The shift register starts to read out the signal with the high level of ϕst, so the time interval of each ϕst determines the signal accumulation time. The pulsewidth of ϕst must also be longer than 200ns and must be overlapped with ϕ2 for at least 200ns. Moreover, in order to start the shift register normally, ϕ2 must be changed only once from the high level to the low level during the high level of ϕst. The timing diagram for each pulse is shown in Figure. 5.

• End of Scan ($\overline{EOS}$)

By wiring the $\overline{EOS}$ terminal at 5V using a pull-up resistor of 10kΩ, the end of scan signal is obtained, being synchronized with the ϕ2 timing right after the last photodiode is addressed.

Figure 5: Timing Diagram for Drive Circuit



• Signal Readout Circuit

The S3921 and S3924 series MOS linear image sensors include a signal processing circuit which integrates a signal charge in the video line and performs impedance conversion to provide output signal with boxcar waveform. This allows signal readout with a simple external circuit. However, a positive bias must be applied to the video line because the photodiode anode of MOS linear image sensors is at 0V (V_{SS}). This is done by adding an appropriate pulse to the reset ϕ terminal. The amplitude of the reset pulse (reset ϕ) should be equal to ϕ1, ϕ2 and ϕst.

When the reset pulse is at the high level, the video line is set at the reset voltage. Figure 6 shows the reset voltage margin. Higher supply clock amplitude allows higher reset voltage and saturation charge. Conversely, if the reset voltage is set at a low level with higher supply clock amplitude, the fall time of video output waveform can be shortened. It is recommended that the reset voltage be set at 2.5V when the amplitude of ϕ1, ϕ2, ϕst and reset ϕ is 5V.

The fall of reset ϕ must be prior to the rise of ϕ2 because the photodiode signal is obtained at the rise of

$\phi 2$. To obtain a stable output, an overlap between the reset pulse (reset ϕ) and $\phi 2$ must be settled, and furthermore, the fall edge of reset ϕ should be delayed from the fall edge of $\phi 2$.

The S3921 and S3924 series provide output signal with negative boxcar waveform which includes a DC offset of approximately 1V when the reset voltage is 2.5V. Accordingly, when it is desired that the DC offset is null and the waveform is altered to the positive polarity, the signal readout circuit and pulse timing shown in Figure 7 are recommended. In this circuit, R_S must be larger than 10kΩ. Also, the gain is determined by the ratio of R_f to R_S, so, choose the value of R_f that suits your application.

Hamamatsu provides driver/amplifier circuits; the C4074 specifically designed for the S3921 and S3924 series. In addition, the C4091 pulse generator is available, which supplies the C4074 with a master start pulse and master clock pulse.

Figure 6: Reset Voltage Margin

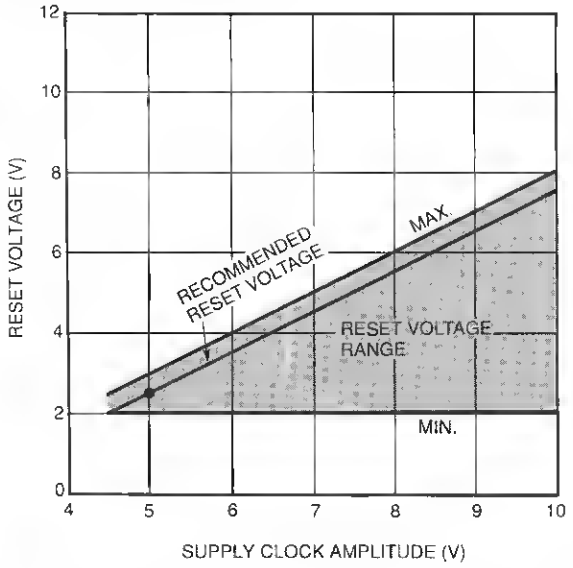
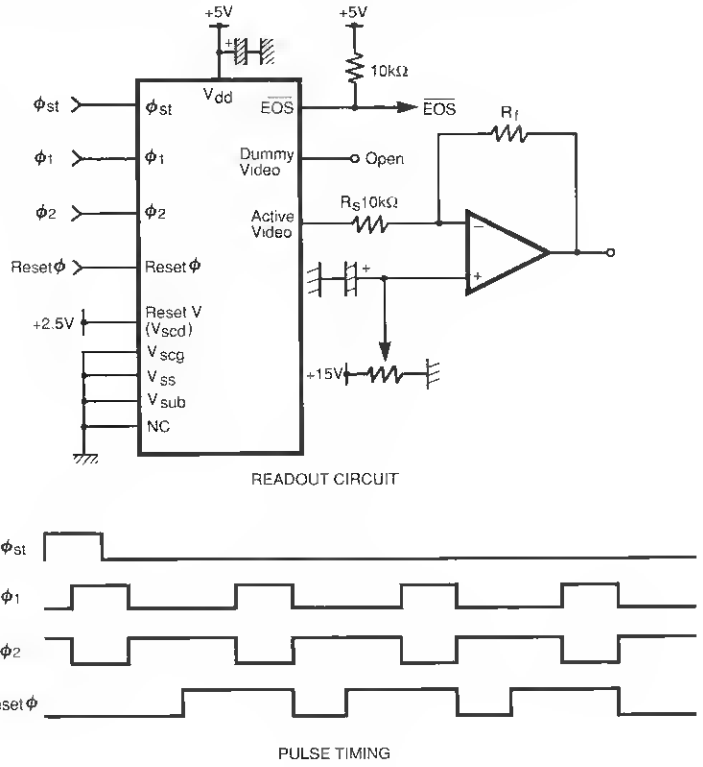


Figure 7: Recommended Readout Circuit and Pulse Timing



• Operation for Saturation Control

When the MOS linear image sensor is used at a light level lower than the saturation exposure, the saturation control function is not necessary. The saturation control drain should be set at a voltage equal to the reset V and the gate should be grounded (0V).

When light higher than the saturation exposure strikes the sensitive area, even partially, the photodiode cannot accumulate a signal charge exceeding the saturation charge amount. The excessive charge begins to overflow into the video line, thus causing deterioration of the signal purity. In order to eliminate this phenomenon, a voltage equal to the reset V (typically 2.5V) should be given to the saturation control drain. Also, a bias voltage should be applied to the saturation control gate so that the saturation charge amount is set at the desired level. The larger the bias voltage for the saturation control gate, the higher the saturation control function will be. However, a larger bias voltage also causes a decrease in the saturation charge amount. Therefore, it is necessary to select the appropriate bias voltage value carefully.

APPENDIX

1) **Operation for all photodiode reset:**
In normal operation, the charge accumulated in the photodiode is reset when the signal is read out. For the S3921 and S3924 series, the signal charge can be reset at a line other than the signal readout. This is done by adding an appropriate pulse to the saturation control gate. The amplitude of this pulse should be equal to $\phi 1$, $\phi 2$, ϕst and reset ϕ, and the pulsewidth should be longer than 5µs.

When the saturation control gate is set at the high level, all photodiodes are reset simultaneously at the potential of the saturation control drain. (This is set at the same potential as the reset V and is typically 2.5V.) On the contrary, when the saturation control gate is set at the low level, the signal charge accumulates in the photodiode without a reset being carried out.

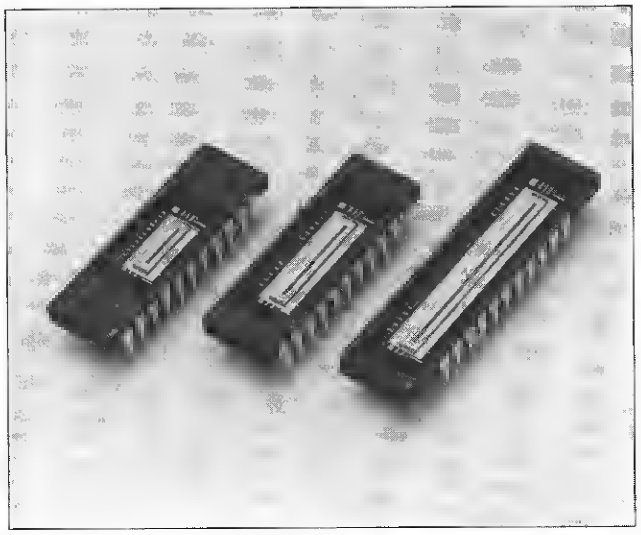
2) **Dummy video:**
The S3921 and S3924 series have a dummy video line for altering the output polarity to positive and for eliminating the DC offset in the video output waveform. Video signal with no DC offset and with positive polarity can be obtained by the differential amplification between the active video line and dummy video line outputs. But, in normal operation, the dummy video line need not to be used. Leave it unconnected.

HAMAMATSU

TECHNICAL DATA

SERIAL/VOLTAGE OUTPUT TYPE MOS LINEAR IMAGE SENSORS S3922, S3923 SERIES

High UV Sensitivity, 0.5mm Photodiode Height, Integrated Signal Processing Circuit Provides Boxcar Output Waveform



FEATURES

- **Integrated signal processing circuit provides boxcar output waveform for simple readout**
- **Medium wide photosensitive area**
  Photodiode pitch : 50μm (S3922), 25μm (S3923)
  Photodiode height : 0.5mm
- **High UV sensitivity with good stability**
- **Excellent photometric capabilities**
  Low dark current and high saturation charge
  Wide dynamic range
- **Operatable with low voltage, single power supply**
- **Low power consumption**
- **Start pulse, clock pulses and video-line reset pulse are CMOS logic compatible**

APPLICATIONS

- **Multichannel spectrophotometry**
- **Image readout systems**

DESCRIPTION

By applying NMOS technology to the manufacture of self-scanning linear photodiode arrays, Hamamatsu can offer higher performance and increased flexibility to photometric instrument manufacturers. The new design achieves high UV sensitivity without deterioration even by extended UV exposure. Application is simplified because of single supply operation, low power consumption, and single video output line. All members of the series are pin compatible.

The S3922 and S3923 MOS linear image sensors feature a signal processing circuit which integrates a signal charge in the video line and performs impedance conversion to provide output signal with boxcar waveform. This allows signal readout with a simple external circuit. The S3922 and S3923 also have a wide photosensitive area of 0.5mm photodiode height and 50μm (S3922) or 25μm (S3923) photodiode pitch.

Figure 1: Equivalent Circuit

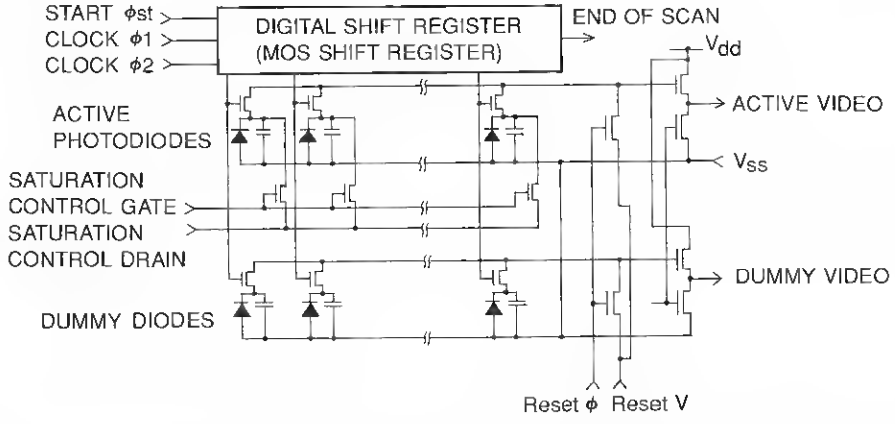
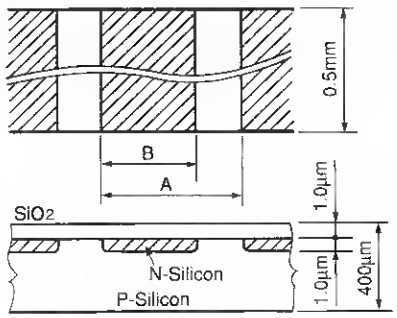


Figure 2: Sensor Geometry



S3922: A=50μm, B=45μm
S3923: A=25μm, B=20μm

MAXIMUM RATINGS

Parameters	Symbols	S3922, S3923	Units
Supply Voltage	V_{dd}	15	V
Supply Clock Amplitude	$V\phi$	15	V
Qperating Temperature ①	Topr	−40 to +65	°C
Storage Temperature	Tstg	−40 to +85	°C

① No dew

ELECTRICAL CHARACTERISTICS (Ta=25°C)

Parameters	Symbols	S3922 Series			S3923 Series			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage for Source Follower Circuit ①	V_{dd}	4.5	$V\phi$	10	4.5	$V\phi$	10	V
Reset Voltage (Reset V) ②	V_r	2.0	$V\phi$−2.5	$V\phi$−2.0	2.0	$V\phi$−2.5	$V\phi$−2.0	V
Saturation Control Gate Voltage	Vscg	—	0	—	—	0	—	V
Saturation Control Drain Voltage ②	Vscd	—	V_r	—	—	V_r	—	V
Start Pulse Voltage (ϕst) ① -High	$V\phi s(H)$	4.5	$V\phi$	10	4.5	$V\phi$	10	V
-Low	$V\phi s(L)$	0	—	0.4	0	—	0.4	V
Clock Pulse Voltage (ϕ1, ϕ2) -High	$V\phi1$, $V\phi2(H)$	4.5	5	10	4.5	5	10	V
-Low	$V\phi1$, $V\phi2(L)$	0	—	0.4	0	—	0.4	V
Reset Pulse Voltage (Reset ϕ) ① -High	$V_{r\phi}(H)$	4.5	$V\phi$	10	4.5	$V\phi$	10	V
-Low	$Vr\phi(L)$	0	—	0.4	0	—	0.4	V
Start Pulse Rise/Fall Times (ϕst)	$t_{r\phi s}$, $t_{f\phi s}$	—	—	500	—	—	500	ns
Start Pulsewidth (ϕst)	$t_{pw\phi s}$	200	—	—	200	—	—	ns
Clock Pulse Rise/Fall Times (ϕ1, ϕ2)	$t_{r\phi1}$, $t_{r\phi2}$, $t_{f\phi1}$, $t_{f\phi2}$	—	—	500	—	—	500	ns
Clock Pulsewidth (ϕ1, ϕ2)	$t_{pw\phi1}$, $t_{pw\phi2}$	200	—	—	200	—	—	ns
Reset Pulse Rise/Fall Times	$t_{rr\phi}$, $t_{fr\phi}$	—	—	500	—	—	500	ns
Start Pulse (ϕst) and Clock Pulse (ϕ2) Qverlap	$t_{\phi ov}$	200	—	—	200	—	—	ns
Clock Pulse (ϕ2) and Reset Pulse (Reset ϕ) Qverlap	$t_{\phi ovr}$	660	—	—	660	—	—	ns
Clock Pulse (ϕ2) to Reset Pulse (Reset ϕ) Delay Time	$t_{d\phi r-2}$	50	—	—	50	—	—	ns
Clock Pulse Space (ϕ1, ϕ2)	X1, X2	0	—	—	0	—	—	ns
Clock Pulse Space (ϕ2, Reset ϕ)	$t_{s\phi r-2}$	0	—	—	0	—	—	ns
Data Rate	f	0.1	—	500	0.1	—	500	kHz
Video Delay Time (50% of saturation)	t_{vd}	—	100 (-128Q) –		—	100 (-256Q) –		ns
		—	150 (-256Q) –		—	150 (-512Q) –		ns
		—	200 (-512Q) –		—	200 (-1024Q) –		ns
Clock Pulse Line Capacitance (ϕ1, ϕ2) at 5V bias	$C\phi$	—	20 (-128Q) –		—	26 (-256Q) –		pF
		—	37 (-256Q) –		—	50 (-512Q) –		pF
		—	72 (-512Q) –		—	93 (-1024Q) –		pF
Reset Pulse Line Capacitance (Reset ϕ) at 5V bias	C_r	—	6	—	—	6	—	pF
Qutput Impedance at V_{dd}=5V, V_r=2.5V	Zo	—	200	—	—	200	—	Ω
Power Consumption at V_{dd} =5V, V_r=2.5	P	—	—	10	—	—	10	mW

① $V\phi$ is supply clock amplitude
② Reset V and saturation control drain use pin 7 in common.

ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

Parameters	Symbols	S3922 Series			S3923 Series			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Photodiode Pitch		—	50	—	—	25	—	μm
Photodiode Height		—	0.5	—	—	0.5	—	mm
Photodiode Dark Current ①	I_d	—	0.1	0.15	—	0.05	0.08	pA
Photodiode Capacitance ①	C_{ph}	—	3.6	—	—	1.8	—	pF
Spectral Response (20% of peak)	λ	200 to 1000			200 to 1000			nm
Wavelength of Peak Response	λp	—	600	—	—	600	—	nm
Saturation Exposure ①	Esat	—	80	—	—	80	—	mlx•s
Saturation Charge ①	Qsat	—	9	—	—	4.5	—	pC
Saturation Output Voltage ①	V_{sat}	—	830 (-128Q) –		—	630 (-256Q) –		mV
		—	600 (-256Q) –		—	400 (-512Q) –		mV
		—	380 (-512Q) –		—	200 (-1024Q) –		mV
Sensitivity Uniformity (50% of saturation, excluding first and last elements)		—	—	±3	—	—	±3	%

① Reset voltage : 2.5V, V_{dd} : 5V, Supply clock amplitude : 5V

Figure 3: Typical Spectral Response

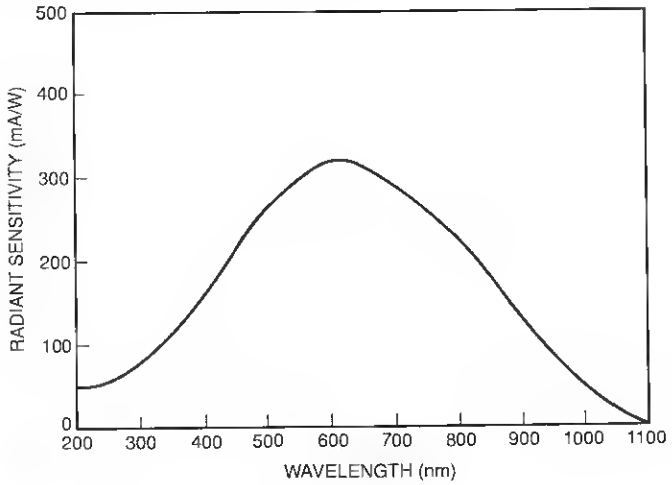
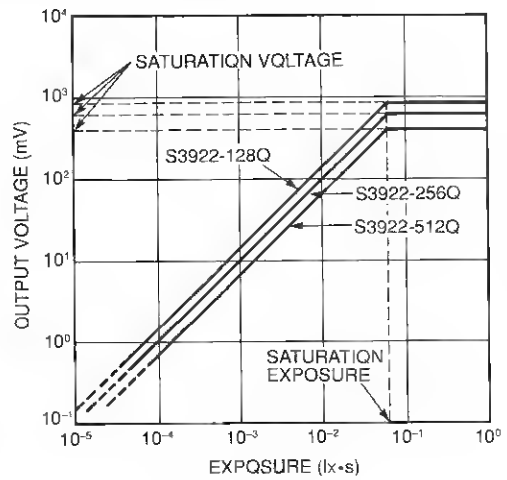
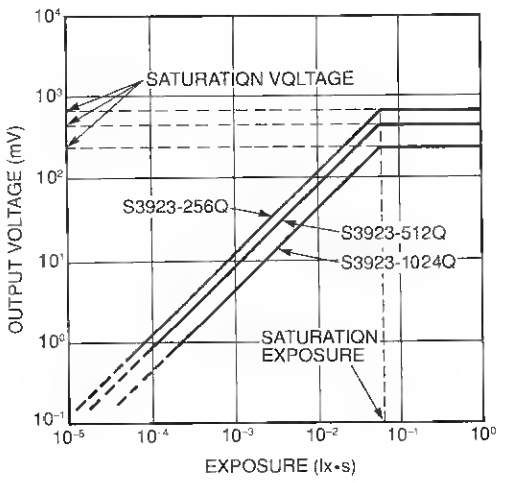


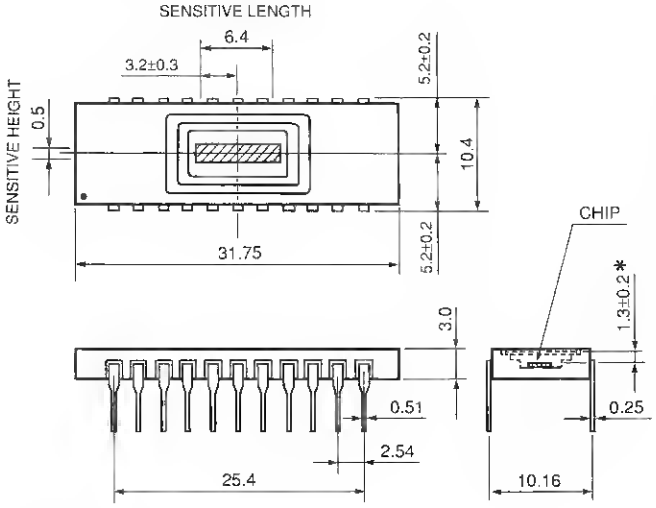
Figure 4: Output Voltage vs. Exposure



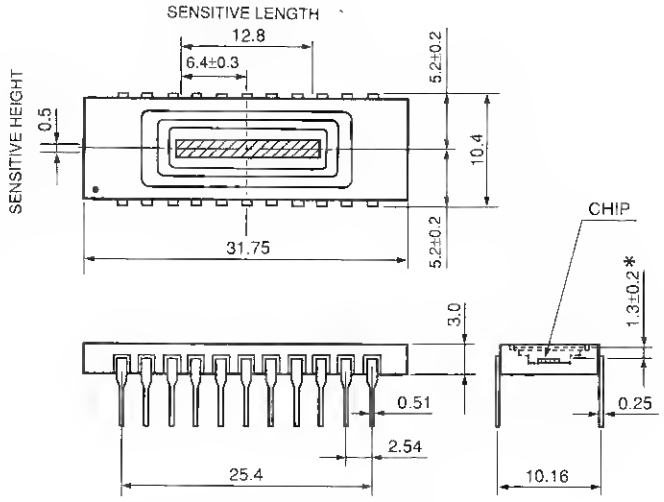


DIMENSIONAL OUTLINES (Unit: mm)

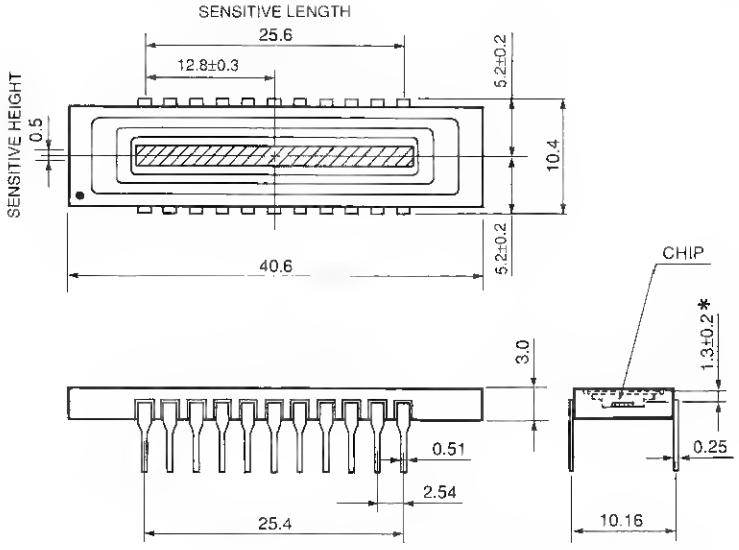
S3922–128Q
S3923–256Q



S3922–256Q
S3923–512Q



S3922–512Q
S3923–1024Q



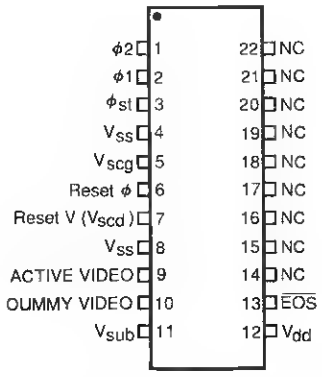
* Optical distance from the outer surface of the quartz window to the chip surface.

• Mechanical Specifications

Parameters	S3922 –128Q	S3922 –256Q	S3922 –512Q	S3923 –256Q	S3923 –512Q	S3923 –1024Q	Units
Number of Photodiodes	128	256	512	256	512	1024	—
Ceramic Length	31.75		40.6	31.75		40.6	mm
Number of Pins	22			22			—
Window Material ①	Quartz			Quartz			—
Net Weight	3.0		3.5	3.0		3.5	g

① Fiber optic window is available.

PINOUT AND RECOMMENDED OPERATING CONDITIONS



V_{ss}, V_{sub} and NC should be grounded.

Terminals	Input or Output	Description
ϕ_1, ϕ_2	Input (CMOS logic compatible)	Pulses for operating the MOS shift register. As the video output signal is obtained being synchronized with the rise of ϕ_2, the video data rate is equal to the clock pulse frequency.
ϕ_{st}	Input (CMOS logic compatible)	Pulse for start operating the MOS shift register. The time interval between start pulses is equal to the signal accumulation time.
V_{ss}	Passive node	Connected with the anode of each photodiode. This should be grounded.
V_{scg}	Input	Used for restricting blooming. This shoud be grounded when it is not necessary.
Reset ϕ	Input (CMOS logic compatible input)	With the high level, the video line is reset at Reset V voltage.
Reset V	Input	A positive voltage should be applied to the video line connecting with photodiode cathodes so that each photodiode is reverse-biased. It is recommended that Reset V be 2.5V when the amplitude of ϕ_1, ϕ_2, ϕst and Reset ϕ is 5V. Reset V and Vscd use pin 7 in common.
V_{scd}	Input	Used for restricting blooming. This should be biased at a voltage equal to Reset V even when it is not necessary.
ACTIVE VIDEO	Output	Low-impedance video output signal after internal current-voltage conversion. Negative polarity output including a DC offset.
DUMMY VIDEO	Output	This has the same structure as the active video, but is not connected with photodiodes, so only DC offset is output. Open circuit when it is not necessary.
V_{sub}	Passive node	Connected with the silicon substrate. This should be grounded.
V_{dd}	Input	Supply voltage to the internal impedance conversion circuit. It should be biased at a voltage equal to the amplitude of each clock (typically 5V).
$\overline{EOS}$	Output (CMOS logic compatible)	This should be pulled up at 5V using a 10kΩ resistor. Negative polarity. This is obtained synchronously with the ϕ_2 timing right after the last photodiode is addressed.
NC		No connection. These should be grounded.

DRIVER CIRCUIT

• Driver Circuit

Driving the MOS shift register requires a start pulse (ϕst) and two-phase clock pulses (ϕ1, ϕ2). The polarities of ϕst, ϕ1 and ϕ2 are positive and these pulses are CMOS logic compatible.

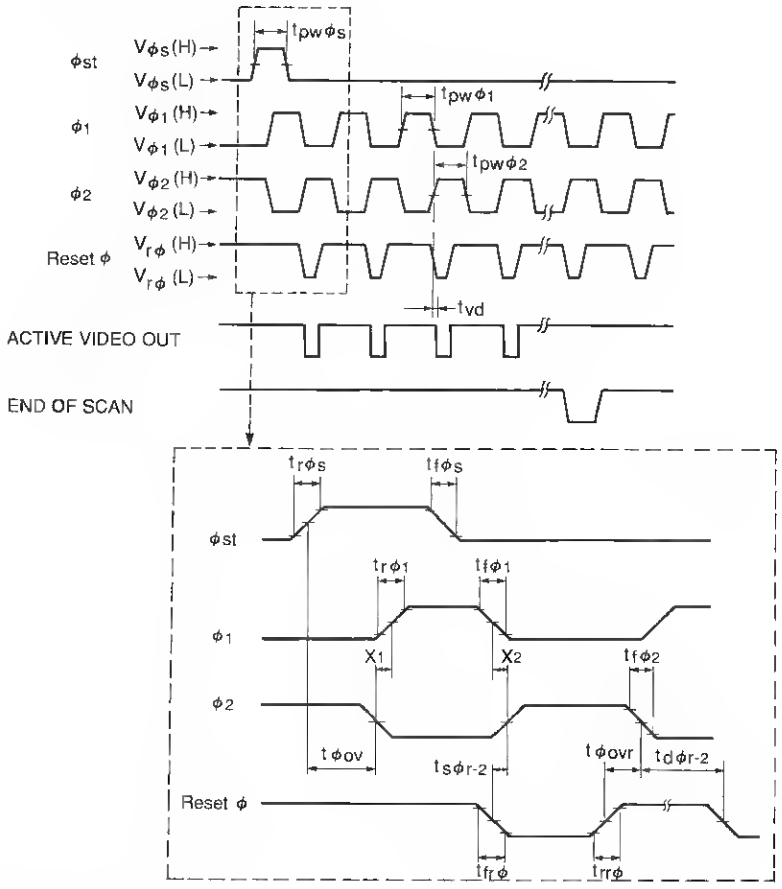
ϕ1 and ϕ2 can be either fully separated or in the complementary relation. However, the overlap should not exceed 50% of the rise or fall edge between ϕ1 and ϕ2. The pulsewidth of ϕ1 and ϕ2 must be longer than 200 ns. Since the photodiode signal is obtained at the rise of every ϕ2, the clock pulse frequency determines the video data rate.

The amplitude of ϕst should be equal to that of ϕ1 and ϕ2. The shift register starts to read out the signal with the high level of ϕst, so the time interval of each ϕst determines the signal accumulation time. The pulsewidth of ϕst must also be longer than 200ns and must be overlapped with ϕ2 for at least 200ns. Moreover, in order to start the shift register normally, ϕ2 must be changed only once from the high level to the low level during the high level of ϕst. The timing diagram for each pulse is shown in Figure. 5.

• End of Scan ($\overline{\text{EOS}}$)

By wiring the $\overline{\text{EOS}}$ terminal at 5V using a pull-up resistor of 10kΩ, the end of scan signal is obtained, being synchronized with the ϕ2 timing right after the last photodiode is addressed.

Figure 5: Timing Diagram for Drive Circuit



• Signal Readout Circuit

The S3922 and S3923 series MOS linear image sensors include a signal processing circuit which integrates a signal charge in the video line and performs impedance conversion to provide output signal with boxcar waveform. This allows signal readout with a simple external circuit. However, a positive bias must be applied to the video line because the photodiode anode of MOS linear image sensors is at 0V (V_{SS}). This is done by adding an appropriate pulse to the reset ϕ terminal. The amplitude of the reset pulse (reset ϕ) should be equal to ϕ1, ϕ2 and ϕst.

When the reset pulse is at the high level, the video line is set at the reset voltage. Figure 6 shows the reset voltage margin. Higher supply clock amplitude allows higher reset voltage and saturation charge. Conversely, if the reset voltage is set at a low level with higher supply clock amplitude, the fall time of video output waveform can be shortened. It is recommended that the reset voltage be set at 2.5V when the amplitude of ϕ1, ϕ2, ϕst and reset ϕ is 5V.

The fall of reset ϕ must be prior to the rise of ϕ2 because the photodiode signal is obtained at the rise of

$\phi 2$. To obtain a stable output, an overlap between the reset pulse (reset ϕ) and $\phi 2$ must be settled, and furthermore, the fall edge of reset ϕ should be delayed from the fall edge of $\phi 2$.

The S3922 and S3923 series provide output signal with negative boxcar waveform which includes a DC offset of approximately 1V when the reset voltage is 2.5V. Accordingly, when it is desired that the DC offset is null and the waveform is altered to the positive polarity, the signal readout circuit and pulse timing shown in Figure 7 in Figure 7 are recommended. In this circuit, R_S must be larger than 10kΩ. Also, the gain is determined by the ratio of R_f to R_S , so, choose the value of R_f that suits your application.

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Figure 6: Reset Voltage Margin

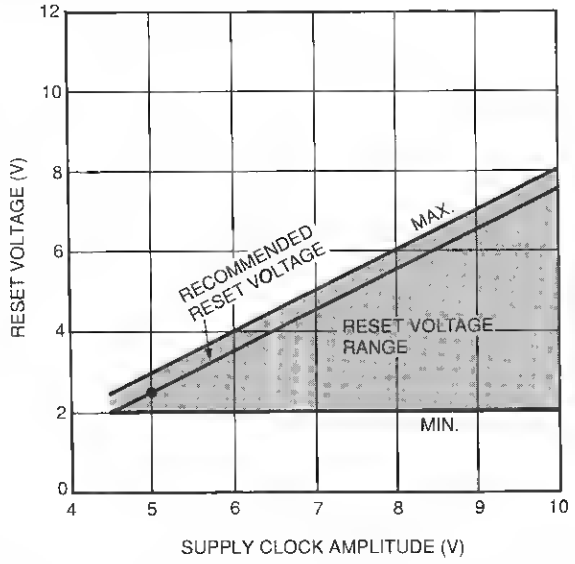
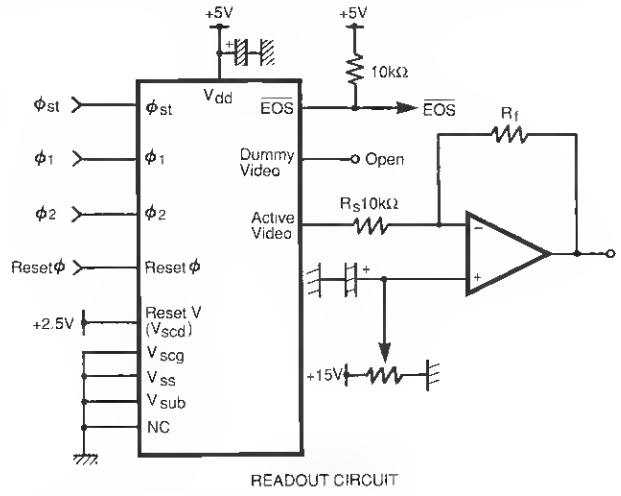


Figure 7: Recommended Readout Circuit and Pulse Timing



• Operation for Saturation Control

When the MOS linear image sensor is used at a light level lower than the saturation exposure, the saturation control function is not necessary. The saturation control drain should be set at a voltage equal to reset V and the gate should be grounded (0V).

When light higher than the saturation exposure strikes the sensitive area, even partially, the photodiode cannot accumulate a signal charge exceeding the saturation charge amount. The excessive charge begins to overflow into the video line, thus causing deterioration of the signal purity. In order to eliminate this phenomenon, a voltage equal to the reset V (typically 2.5V) should be given to the saturation control drain. Also, a bias voltage should be applied to the saturation control gate so that the saturation charge amount is set at the desired level. The larger the bias voltage for the saturation control gate, the higher the saturation control function will be. However, a larger bias voltage also causes a decrease in the saturation charge amount. Therefore, it is necessary to select the appropriate bias voltage value carefully.

APPENDIX

1) **Operation for all reset:**
In normal operation, the charge accumulated in the photodiode is reset when the signal is read out. For the S3922 and S3923 series, the signal charge can be reset at a line other than the signal readout. This is done by adding an appropriate pulse to the saturation control gate. The amplitude of this pulse should be equal to $\phi 1$, $\phi 2$, ϕ st and reset ϕ, and the pulsewidth should be longer than 5µs.

When the saturation control gate is set at the high level, all photodiodes are reset at once at the potential of the saturation control drain. (This is set at the same potential as the reset V, and is typically 2.5V.) On the contrary, when the saturation control gate is set at the low level, the signal charge accumulates in the photodiode without a reset being carried out.

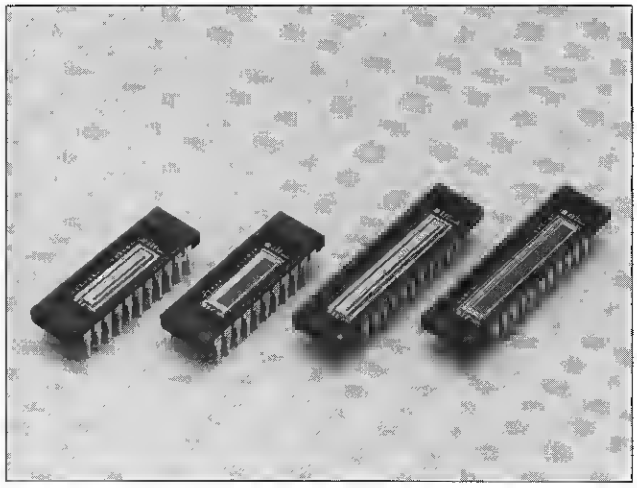
2) **Dummy video:**
The S3922 and S3923 series have a dummy video line for altering the output polarity to positive and for eliminating the DC offset in the video output waveform. Video signal with no DC offset and with positive polarity can be obtained by differential amplification between the active video line and dummy video line output. But, in normal operation, the dummy video line need not to be used. Leave it unconnected.

HAMAMATSU

TECHNICAL DATA

RANDOM ADDRESS TYPE MOS LINEAR IMAGE SENSORS S3900, S3906 SERIES

Wide Sensitive Area (2.5mm or 0.5 mm Photodiode Height), High UV Sensitivity, Random Address Readout Offers Highly Flexible Measurements



FEATURES

- **Random address readout**
- **Employs the same package as serial readout types**
- **Wide photosensitive area**
  - **Photodiode pitch : 25μm**
  - **Photodiode height : 2.5mm (S3900), 0.5mm (S3906)**
- **High UV sensitivity with good stability**
- **Excellent photometric capabilities**
  - **Low dark current and high saturation charge**
  - **Good linearity**
  - **Wide dynamic range**
- **Operatable with low voltage, single power supply**
- **Low power consumption**
- **Clock pulses and input address pulses are CMOS logic compatible**

APPLICATIONS

- **Multichannel spectrophotometry**
- **Image readout systems**

DESCRIPTION

By applying NMOS technology to the manufacture of linear photodiode arrays, Hamamatsu can offer higher performance and increased flexibility to photometric instrument manufacturers. The new design achieves high UV sensitivity without deterioration even by extended UV exposure. In addition, the random address types allow the user to read out any of desired elements.

The S3900 and S3906 series random address MOS linear image sensors include a decoder circuit which turns on a desired address switch by adding three-phase clock pulses and input address pulses. The S3900 series has a wide photosensitive area of 2.5mm photodiode height, while the S3906 series is 0.5mm. Both series offers 25μm photodiode pictch.

Figure 1: Equivalent Circuit

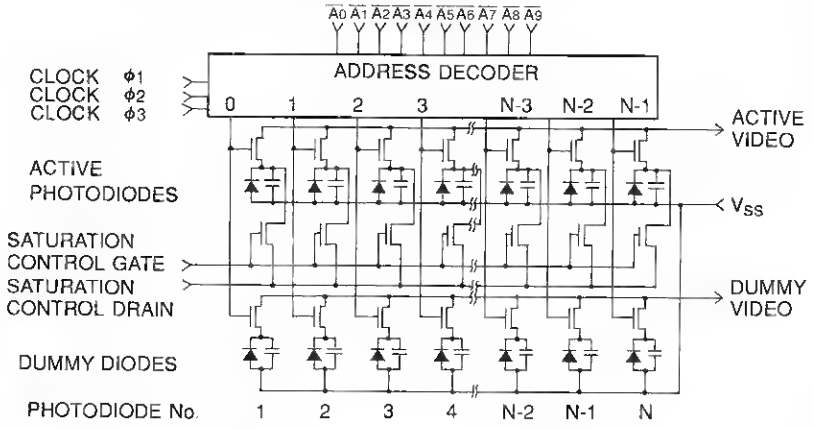
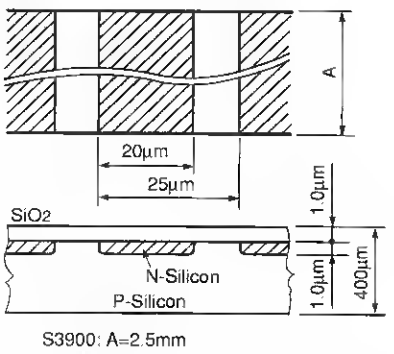


Figure 2: Sensor Geometry



S3900: A=2.5mm
S3906: A=0.5mm

MAXIMUM RATINGS

Parameters	Symbols	S3900, S3906	Units
Supply Voltage	V_{dd}	15	V
Supply Clock Amplitude	$V\phi$	15	V
Operating Temperature ①	Topr	−40 to +65	°C
Storage Temperature	Tstg	−40 to +85	°C

① No dew

ELECTRICAL CHARACTERISTICS (Ta=25°C)

Parameters	Symbols	S3900 Series			S3906 Series			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage to address decoder ①	V_{dd}	4.5	$V\phi$	10	4.5	$V\phi$	10	V
Video Bias Voltage ①	V_b	1.5	$V\phi$–3.0	$V\phi$–2.5	1.5	$V\phi$–3.0	$V\phi$–2.5	V
Saturation Control Gate Voltage	V_{scg}	—	0	—	—	0	—	V
Saturation Control Drain Voltage	V_{scd}	—	V_b	—	—	V_b	—	V
Clock Pulse Voltage ($\phi1$, $\phi2$, $\phi3$) -High	$V\phi1$, $V\phi2$, $V\phi3$ (H)	4.5	5	10	4.5	5	10	V
($\phi1$, $\phi2$, $\phi3$) -Low	$V\phi1$, $V\phi2$, $V\phi3$ (L)	0	—	0.4	0	—	0.4	V
Input Address Pulse Voltage ① -High	$V_{\phi a}$(H)	4.5	$V\phi$	10	4.5	$V\phi$	10	V
($\overline{A0}$-$\overline{A9}$) -Low	$V_{\phi a}$(L)	0	—	0.4	0	—	0.4	V
Clock Pulse Rise/Fall Times ($\phi1$, $\phi2$, $\phi3$)	$t_{r\phi1}$, $t_{r\phi2}$, $t_{r\phi3}$ $t_{f\phi1}$, $t_{f\phi2}$, $t_{f\phi3}$	—	—	500	—	—	500	ns
Input Address Pulse Rise/Fall Times (ϕa)	$t_{r\phi a}$, $t_{f\phi a}$	—	—	500	—	—	500	ns
Clock Pulsewidth ($\phi1$)	$t_{pw\phi1}$	100	—	—	100	—	—	ns
($\phi2$)	$t_{pw\phi2}$	200	—	—	200	—	—	ns
($\phi3$)	$t_{pw\phi3}$	300	—	—	300	—	—	ns
Clock Pulse Rise Time Difference (ϕa, $\phi3$)	$t_{rd\phi a\text{-}3}$	100	—	—	100	—	—	ns
Clock Pulse Rise Time Difference ($\phi3$, $\phi2$)	$t_{rd\phi3\text{-}2}$	100	—	—	100	—	—	ns
Clock Pulse Fall Time Difference ($\phi3$, ϕa)	$t_{fd\phi3\text{-}a}$	0	—	—	0	—	—	ns
Clock Pulse Space ($\phi3$, $\phi1$)	$t_{s\phi3\text{-}1}$	0	—	—	0	—	—	ns
($\phi1$, $\phi2$)	$t_{s\phi1\text{-}2}$	0	—	—	0	—	—	ns
Data Rate	f	1	—	1000	1	—	1000	kHz
Video Delay Time (50% of saturation) ②	t_{vd}	—	150 (-512Q) –		—	120 (-512Q) –		ns
		—	200 (-1024Q) –		—	160 (-1024Q) –		
Clock Pulse Line Capacitance ($\phi1$, $\phi2$, $\phi3$) at 5V bias	$C_{\phi1}$	—	38 (-512Q) –		—	38 (-512Q) –		pF
		—	75 (-1024Q) –		—	75 (-1024Q) –		pF
	$C_{\phi2}$	—	38 (-512Q) –		—	38 (-512Q) –		pF
		—	75 (-1024Q) –		—	75 (-512Q) –		pF
	$C_{\phi3}$	—	31 (-512Q) –		—	31 (-512Q) –		pF
		—	58 (-1024Q) –		—	58 (-1024Q) –		pF
Input Address Pulse Line Capacitance	$C_{\phi a}$	—	12 (-512Q) –		—	12 (-512Q) –		pF
		—	20 (-1024Q) –		—	20 (-1024Q) –		pF
Video Line Capacitance at 2V bias	C_v	—	14 (-512Q) –		—	14 (-512Q) –		pF
		—	27 (-1024Q) –		—	27 (-1024Q) –		pF
Power Consumption at $V\phi$ =5V	P	—	35 (-512Q) –		—	35 (-512Q) –		mW
		—	40 (-1024Q) –		—	40 (-1024Q) –		mW

① $V\phi$ is supply clock amplitude
② Measured with a current-voltage conversion circuit with R_f = 25kΩ.

ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

Parameters	Symbols	S3900 Series			S3906 Series			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Photodiode Pitch		—	25	—	—	25	—	μm
Photodiode Height		—	2.5	—	—	0.5	—	mm
Photodiode Dark Current	I_d	—	0.2	0.3	—	0.05	0.08	pA
Photodiode Capacitance ①	C_{ph}	—	10	—	—	2	—	pF
Spectral Response (20% of peak)	λ	200 to 1000			200 to 1000			nm
Wavelength of Peak Response	λp	—	600	—	—	600	—	nm
Saturation Exposure ①	E_{sat}	—	80	—	—	80	—	mlx•s
Saturation Charge ①	Q_{sat}	—	20	—	—	4	—	V
Sensitivity Uniformity (50% of saturation, excluding first and last elements)		—	—	±10	—	—	±10	%

① Video bias voltage: 2.0V, Supply clock amplitude: 5.0V

Figure 3: Typical Spectral Response

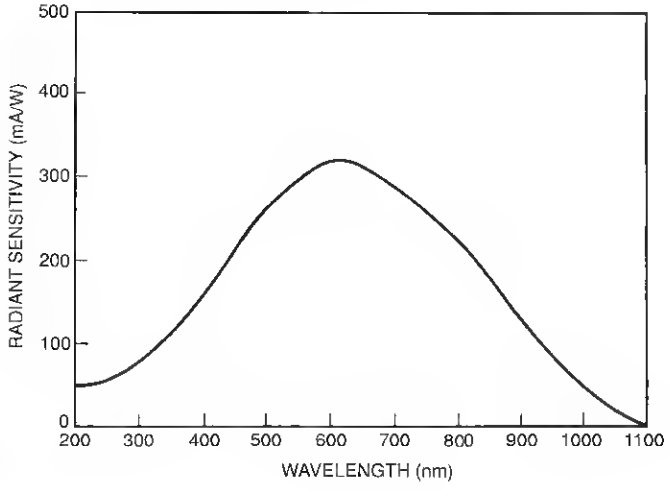
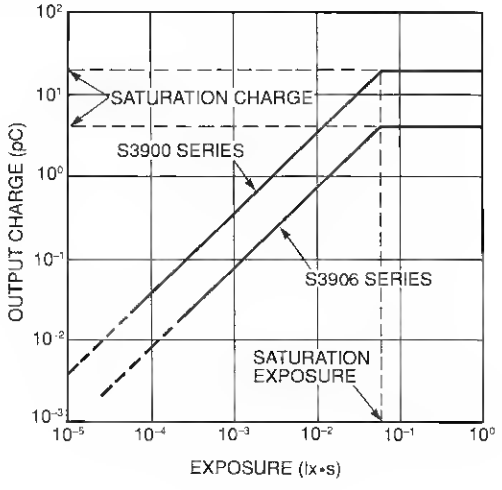
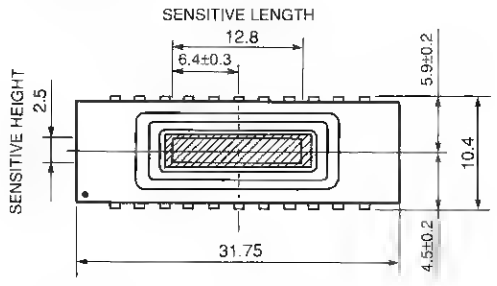


Figure 4: Output Charge vs. Exposure

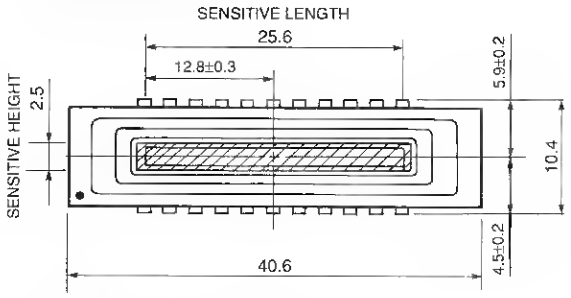


DIMENSIONAL OUTLINES (Unit: mm) AND ADDRESS CODE

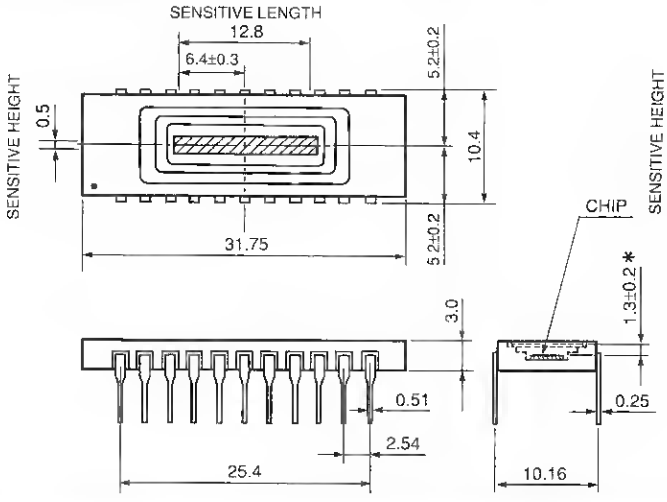
S3900-512Q



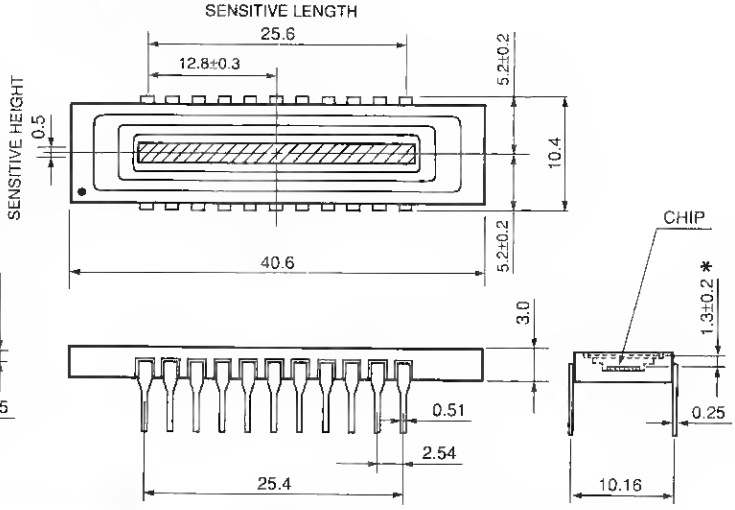
S3900-1024Q



S3906-512Q



S3906-1024Q



* Optical distance from the outer surface of the quartz window to the chip surface.

• Address Code and Photodiode No.

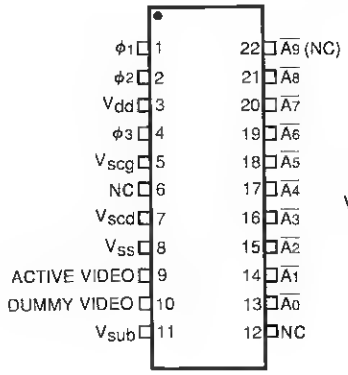
Address	Photodiode No.	$\overline{A0}$	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$
0	1	1	1	1	1	1	1	1	1	1	1
1	2	0	1	1	1	1	1	1	1	1	1
2	3	1	0	1	1	1	1	1	1	1	1
3	4	0	0	1	1	1	1	1	1	1	1
⋮	⋮										
9	10	0	1	1	0	1	1	1	1	1	1
10	11	1	0	1	0	1	1	1	1	1	1
⋮	⋮										
99	100	0	0	1	1	1	0	0	1	1	1
100	101	1	1	0	1	1	0	0	1	1	1
⋮	⋮										
499	500	0	0	1	1	0	0	0	0	0	1
500	501	1	1	0	1	0	0	0	0	0	1
⋮	⋮										
1023	1024	0	0	0	0	0	0	0	0	0	0

• Mechanical Specifications

Parameters	S3900 –512Q	S3900 –1024Q	S3906 –512Q	S3906 –1024Q	Units
Number of Photodiodes	512	1024	512	1024	—
Ceramic Length	31.75	40.6	31.75	40.6	mm
Number of Pins	22		22		—
Window Material ①	Quartz		Quartz		—
Net Weight	3.0	3.5	3.0	3.5	g

① Fiber optic window is available.

PINOUT AND RECOMMENDED OPERATING CONDITION



V_{SS}, V_{sub} and NC should be grounded.

Terminals	Input or Output	Description
$\phi 1$, $\phi 2$, $\phi 3$	Input (CMOS logic compatible)	Pulses for operating the MOS decoder. As the Video output signal is obtained being synchronized with the rise of $\phi 2$, the video output data rate is equal to the clock pulse frequency .
V_{dd}	Input	Supply voltage to the MOS decoder and set at a voltage equal to the amplitude of clock pulses and address pulses.
V_{scg}	Input	Used for restricting blooming. This should be grounded.
V_{scd}	Input	Used for restricting blooming. This should be biased at a voltage equal to the video line even when it is not necessary.
V_{ss}	Passive node	Connected with the anode of each photodiode. This should be grounded.
ACTIVE VIDEO	Output	Video output signal. A positive voltage should be applied to the video line connecting with photodiode cathodes so that each photodiode is reverse-biased. It is recommended that the video bias be 2V when the amplitude of $\phi 1$, $\phi 2$, and $\phi 3$ is 5V.
DUMMY VIDEO	Output	This has the same structure as the active video, but is not connected with photodiodes, so only spike noise is output. It should be biased at a voltage equal to the active video line. Open circuit when it is not necessary.
V_{sub}	Passive node	Connected with the silicon substrate. This should be grounded.
$\overline{A0}$ to $\overline{A9}$	Input (CMOS logic compatible)	Binary code address pulses to select photodiodes to be read out. Negative logic. It is recommended that the rise and fall be synchronized with the positive transition of $\phi 1$. The amplitude of address pulses should be equal to that of clock pulses.
NC		No connection. These should be grounded.

DRIVER CIRCUIT

• Driver Circuit

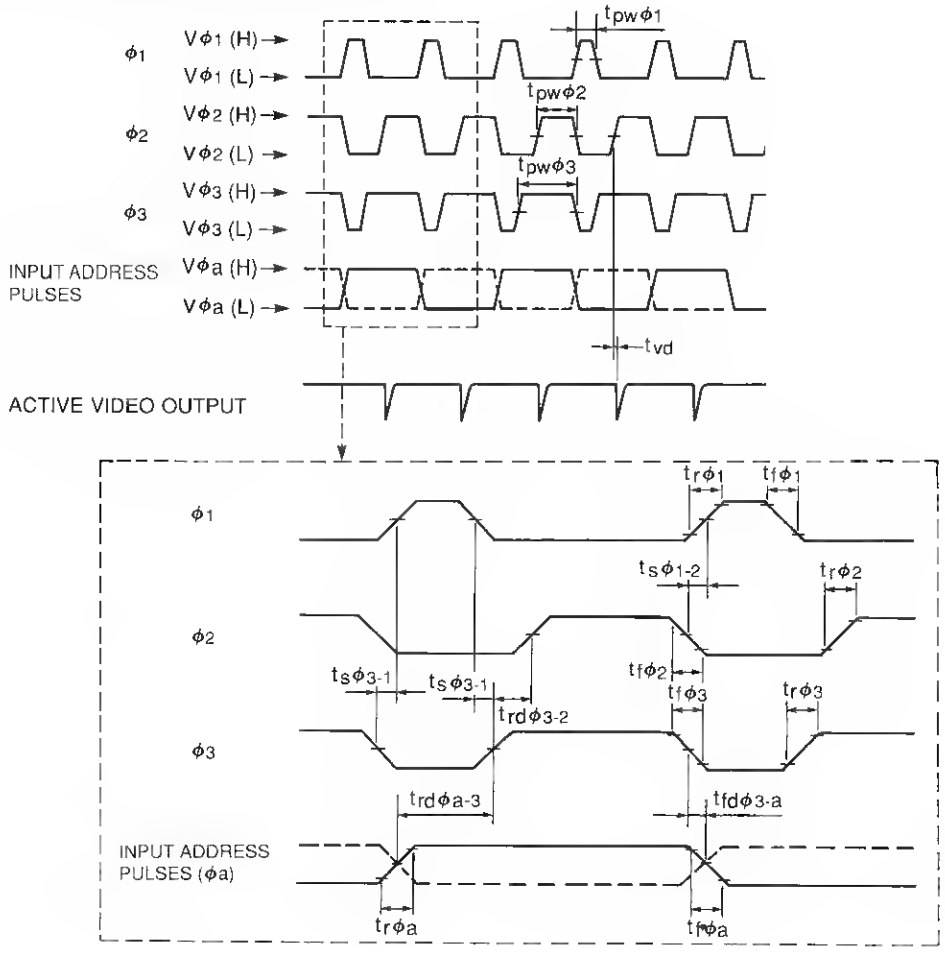
Driving the decoder requires three-phase clock pulses (ϕ1, ϕ2, ϕ3) and also address pulses (ϕa) of binary input which determine the photodiode to be addressed and read out. The applied DC voltage (V_{dd}) and the amplitude of address pulses should be equal to that of clock pulses. The number of input address pulses is 9 for the 512-element type and 10 for the 1024-element type. The polarity of the three-phase clock pulses is positive, but the input address pulses are negative. These pulses are CMOS logic compatible. (For the address code and photodiode No., refer to the previous page.)

ϕ1 and ϕ3 can be either fully separated or in the complementary relation. However, the overlap should not exceed 50% of the rise or fall edge between ϕ1 and ϕ3. The pulsewidth of ϕ1 and ϕ3 must be longer than 100ns and 300ns respectively.

ϕ2 must rise after the rise of ϕ3 with a delay of at least 100ns. Although there is no restriction between the falls of ϕ2 and ϕ3, it is recommended for them to have the simultaneous fall edge. Since the output signal appears synchronized with ϕ2, adjust the ϕ2 pulsewidth according to the signal processing method. The minimum pulsewidth is 200ns.

The input address pulses ϕa must rise prior to the rise of ϕ3 at least 100ns, and also must fall with or after the fall of ϕ3. Accordingly, it is suggested that the rise and fall of ϕa be sychronized with the rise of ϕ1.

Figure 5: Timing Diagram for Drive Circuit



• Signal Readout Circuit

Signal readout methods consist of the current-detection mode using a resistive load and the current-integration mode using a charge amplifier. In either method, a positive bias must be applied to the video line because the photodiode anode of MOS linear image sensors is at 0V (V_{SS}). Figure 6 shows the video bias voltage margin.

Higher supply clock amplitude allows larger video bias and saturation charge. Conversely, if the video bias is set at a low level with higher supply clock amplitude, the fall time of video output waveform can be shortend. It is recommended that the video bias be set at 2V when the amplitude of ϕ1, ϕ2, ϕ3 and ϕa is 5V.

To obtain good output linearity, the current-integration mode is suggested. In this mode, immediately before the each photodiode is addressed each time, the integration capacitance is reset at the reference voltage level (2V), and when the address switch is turned on, the signal charge is accumulated in the integration capacitance. Figure 7 shows an example of the current-integration circuit and the pulse timing. To obtain a stable output , the rise edge of the reset pulse should be delayed at least 50 ns from the fall edge of $\phi 2$.

Hamamatsu provides a driver/amplifier circuit for the current-integration mode; the C4072 specifically designed for random-address MOS linear image sensors.

Figure 6: Video Bias Voltage Margin

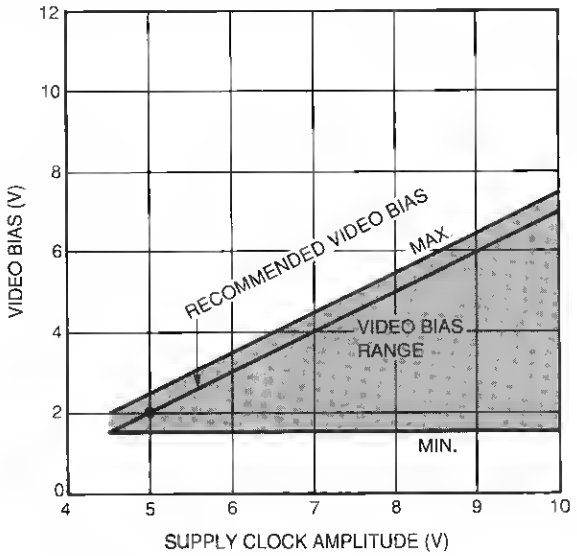
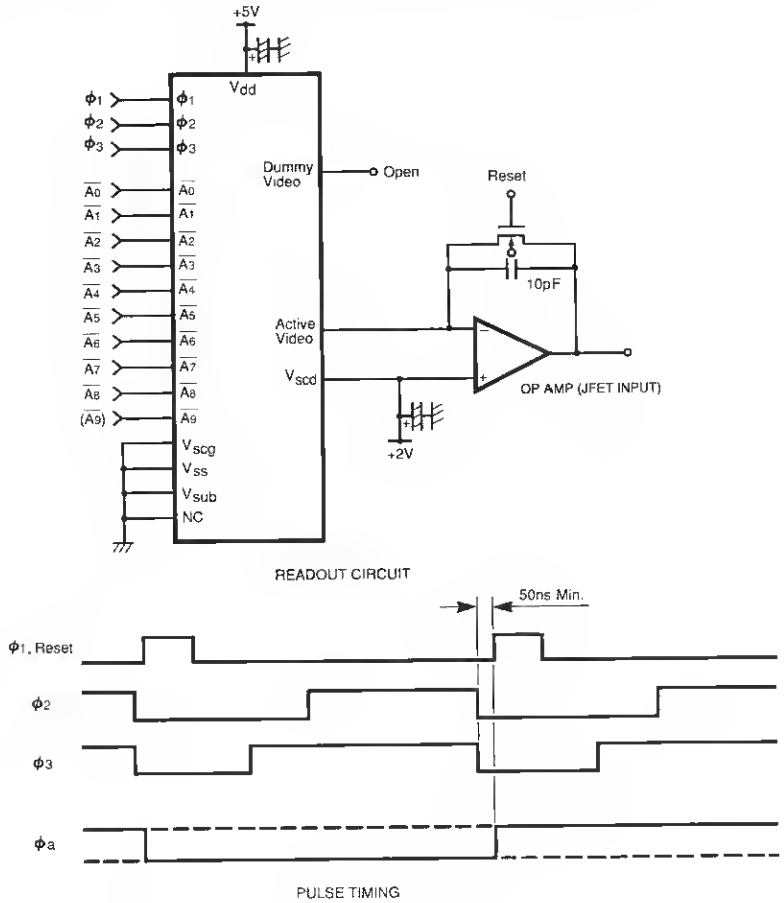


Figure 7: Recommended Readout Circuit and Timing Diagram



• Operation for Saturation Control

When the MOS linear image sensor is used at a light level lower than the saturation exposure, the saturation control function is not necessary. The saturation control drain should be set at a potential equal to the video bias, and the gate should be grounded.

When light higher than the saturation exposure strikes the sensitive area, even partially, the photodiode cannot accumulate a signal charge exceeding the saturation charge amount. The excessive charge begins to overflow into the video line, thus causing deterioration of the signal purity. In order to eliminate this phenomenon, a voltage equal to the video bias (typically 2V) should be given to the saturation control drain. Also, a bias voltage should be applied to the saturation control gate so that the saturation charge amount is set at the desired level. The larger the bias voltage for the saturation control gate, the higher the saturation control function will be. However, a larger bias voltage also causes a decrease in the saturation charge amount. Therefore, it is necessary to select the appropriate bias voltage value carefully.

APPENDIX

1) **Operation for all photodiode reset:**
In normal operation, the charge accumulated in the photodiode is reset when the signal is read out. For the S3900 and S3906 series, the signal charge can be reset at a line other than the signal readout. This is done by adding an appropriate pulse to the saturation control gate. The amplitude of this pulse should be equal to $\phi 1$, $\phi 2$, $\phi 3$ and ϕa, and the pulsewidth should be longer than 5μs.

When the saturation control gate is set at the high level, all photodiodes are reset simultaneously at the potential of the saturation control drain. (This is set at the same potential as the video bias, and is typically 2V.) On the contrary, when the saturation control gate is set at the low level, the signal charge accumulates in the photodiode without a reset being carried out.

2) **Dummy video:**
The S3900 and S3906 series have a dummy video line to eliminate spike noise in the video output waveform. Video signal with lower spike noise can be obtained by the differential amplification between the active video line and dummy video line outputs. But, in normal operation, the dummy video line need not to be used. Leave it unconnected.

HAMAMATSU

TECHNICAL DATA

DRIVER/AMPLIFIER CIRCUIT C4069

For Serial/Current Output Type MOS Linear Image Sensors

The C4069 is a high-speed driver/amplifier circuit designed specifically for use with Hamamatsu serial/current output type MOS linear image sensors (S3901, S3904, S3902, S3903). The C4069 driver/amplifier circuit includes a generator for the start pulse and two-phase clock pulses used to drive a MOS linear image sensor and a signal processing circuitry used to read out the video signal in the current-voltage conversion mode. The signal inputs required are only a master start pulse, master clock pulse and +5V/±15V.

In addition, the C4091 pulse generator is available, which supplies the C4069 with a master start pulse and master clock pulse.

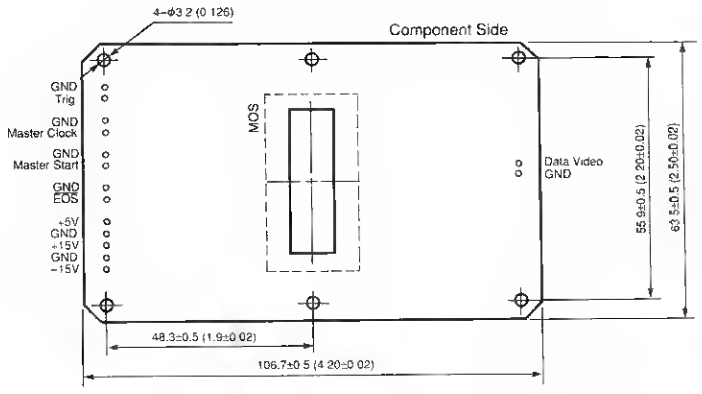
FEATURES

- **Structure allows easy cooling and optical alignment of MOS image sensor**
- **Simple operation: only a master start pulse, a master clock pulse, +5V and ±15V required**
- **High-speed operation (2MHz Max.)**
- **No adjustment**

DESCRIPTIONS OF TERMINALS

	Terminals	Symbols	Descriptions
Input	Supply Voltage	V_d (+5) V_a (+15) (−15)	+5 Vdc, 70 mA +15 Vdc, 30 mA −15 Vdc, 30 mA
Input	Master Start ϕms	St.	CMOS logic compatible. Positive logic. For initializing the circuit and the MOS shift register.
Input	Master Clock ϕmc	CLK	CMOS logic compatible. The maximum frequency 12 MHz. For synchronizing the circuit and the MOS shift register.
Output	Data Video	Video	Positive output. This is the voltage output produced after the current-voltage conversion of the MOS video signal and the differential amplification with respect to the dummy video line. Obtained being synchronized with the positive transition of ϕ2.
Output	Sample-and-hold	Trig.	CMOS logic compatible. Positive logic. This output is used for the trigger signal for the sample-and-hold and A/D conversion.
Output	End of Scan	$\overline{EOS}$	CMOS logic compatible. Negative logic. This is the end-of-scan signal of the MOS shift register and obtained being synchronized with the ϕ2 timing right after the last element is scanned.

Figure 1: Dimensional Outline and Terminals



Dimensions in mm (inches)

Figure 2: Wiring Example

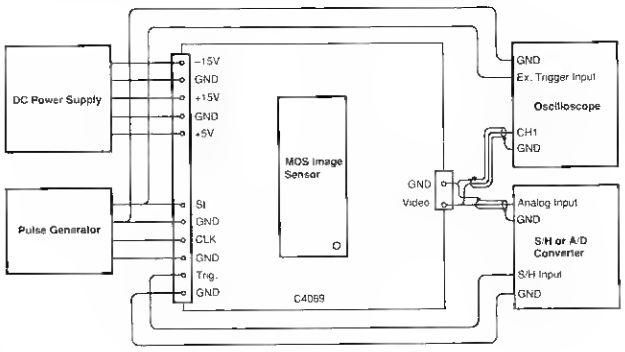


Figure 3: Block Diagram

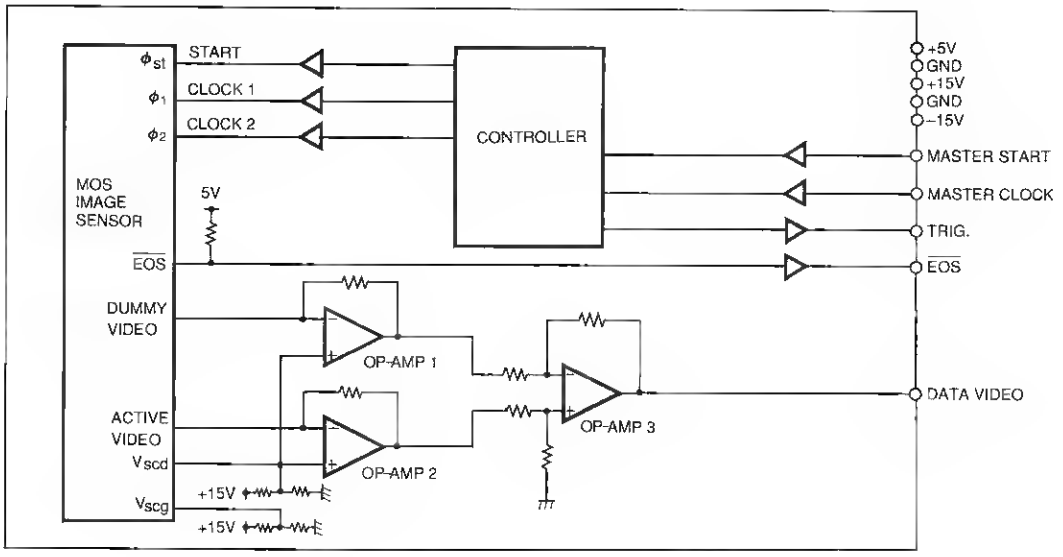
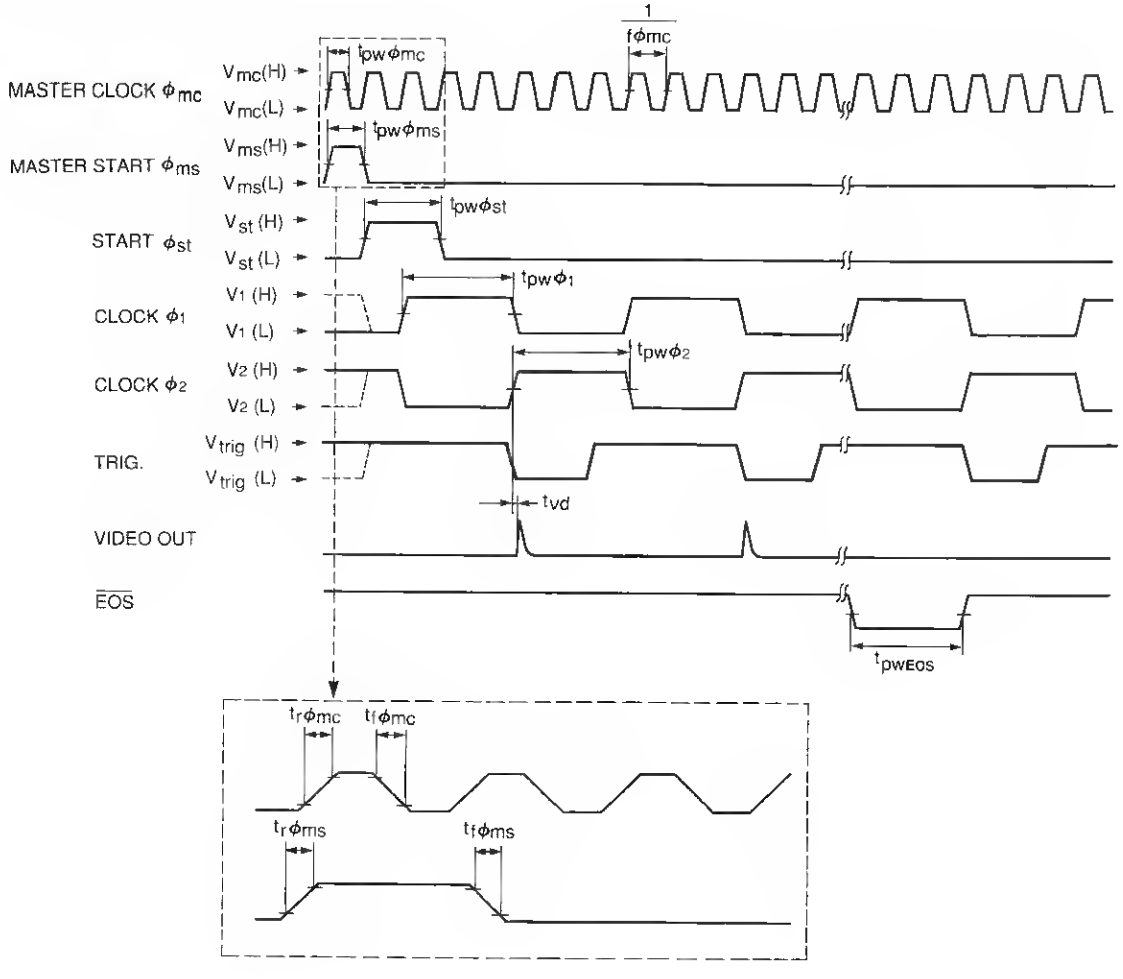


Figure 4: Timing Diagram



HAMAMATSU

TECHNICAL DATA

DRIVER/AMPLIFIER CIRCUIT C4070

For Serial/Current Output Type MOS Linear Image Sensors

The C4070 is a low-noise driver/amplifier circuit designed specifically for use with Hamamatsu serial/current output type MOS linear image sensors (S3901, S3904, S3902, S3903). The C4070 driver/amplifier circuit includes a generator for the start pulse and two-phase clock pulses used to drive a MOS linear image sensor and the charge amplifier used to read out the video signal in the integration mode. The signal inputs required are only a master start pulse, master clock pulse and +5V/±15V.

In addition, the C4091 pulse generator is available, which supplies the C4070 with a master start pulse and master clock pulse.

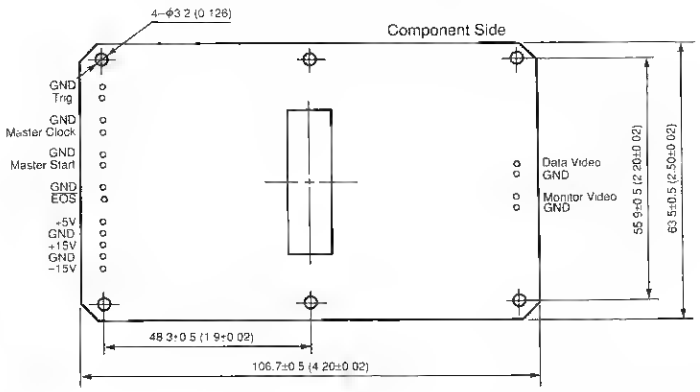
FEATURES

- **Structure allows easy cooling and optical alignment of MOS image sensor**
- **Simple operation: only a master start pulse, a master clock pulse, +5V and ±15V required**
- **Low noise**
- **Wide dynamic range**
- **Simple adjustment**

DESCRIPTIONS OF TERMINALS

	Terminals	Symbols	Descriptions
Input	Supply Voltage	V_d (+5) V_a (+15) (−15)	+5 Vdc, 70 mA +15 Vdc, 30 mA −15 Vdc, 30 mA
Input	Master Start ϕms	St.	CMOS logic compatible. Positive logic. For initializing the circuit and the MOS shift register.
Input	Master Clock ϕmc	CLK	CMOS logic compatible. The maximum frequency 375 kHz. For synchronizing the circuit and the MOS shift register.
Output	Monitor Video	M.V.	Positive output. This is the integrated video signal from the MOS image sensor, and used for monitoring when cancelling the switching noise. Obtained being synchronized with the ϕ2 timing.
Output	Data Video	D.V.	Positive output. This is the integrated, low-noise video signal of an MOS image sensor.
Output	Sample-and-hold	Trig.	CMOS logic compatible. Positive logic. This output is used for the trigger signal for the sample-and-hold and A/D conversion.
Output	End of Scan	$\overline{EOS}$	CMOS logic compatible. Negative logic. This is the end-of-scan signal of the MOS shift register and obtained being synchronized with the ϕ2 timing right after the last element is scanned.

Figure 1: Dimensional Outline and Terminals



Dimensions in mm (inches)

Figure 2: Wiring Example

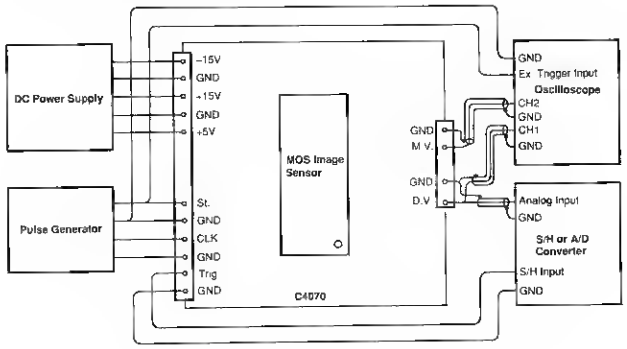


Figure 3: Block Diagram

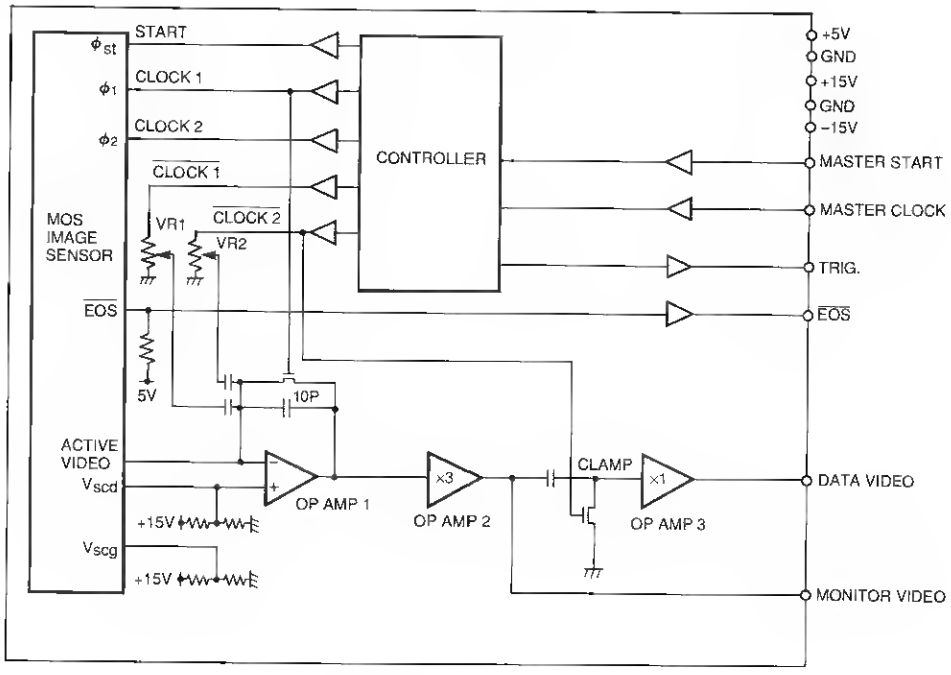
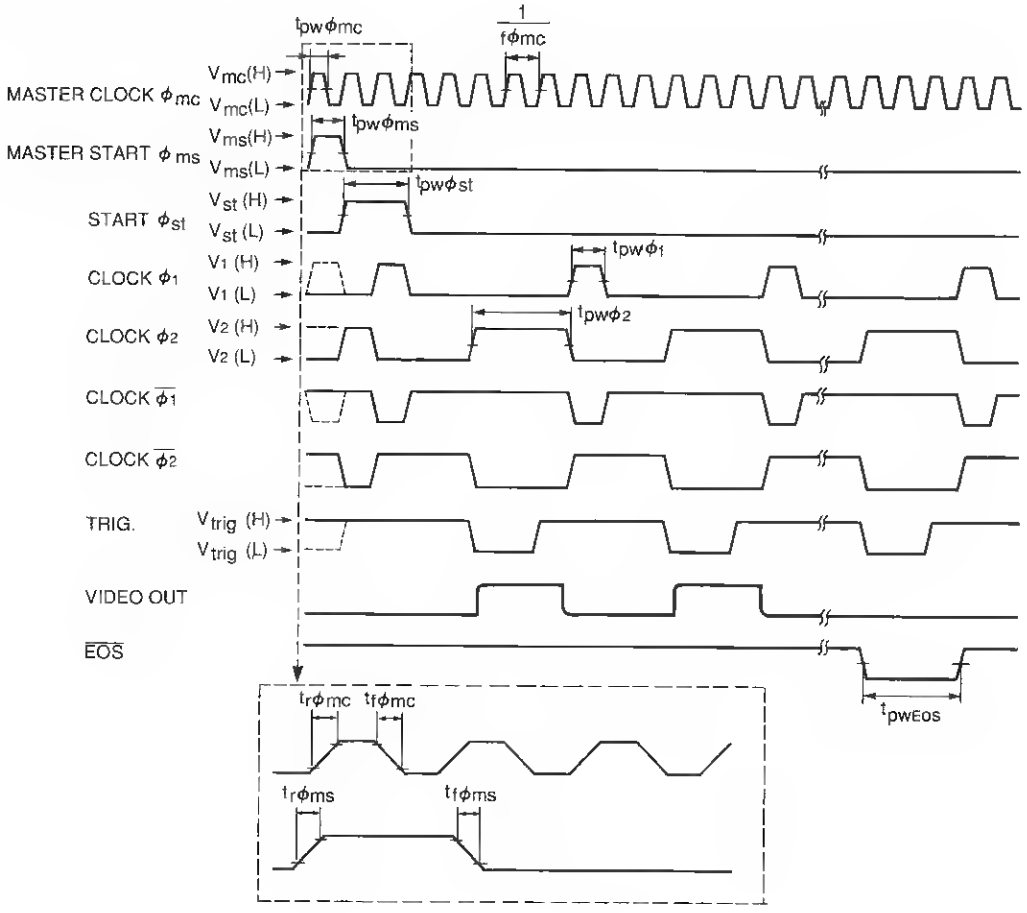


Figure 4: Timing Diagram



HAMAMATSU

TECHNICAL DATA

DRIVER/AMPLIFIER CIRCUIT C4072

For Random Address Type MOS Linear Image Sensors

The C4072 is a driver/amplifier circuit specifically designed for Hamamatsu random address type MOS linear image sensors (S3900, S3906 series). The C4072 driver/amplifier circuit includes a buffer circuit for the input address pulses and input five-phase clock pulses used to drive a MOS linear image sensor and a charge amplifier to read out the video signal in the integration mode. The required signals are input address pulses, clock pulses, and +5V and ±15V.

FEATURES

- **Random address readout is possible by input of binary code address pulses**
- **Structure allows easy cooling and optical alignment of MOS image sensor**
- **Low noise**
- **Wide dynamic range**
- **Simple adjustment**

DESCRIPTIONS OF TERMINALS

	Terminals	Symbols	Descriptions
Input	Supply Voltage	V_d (+5) V_a (+15) (−15)	+5 Vdc, 25 mA +15 Vdc, 30 mA −15 Vdc, 30 mA
Input	Address Pulse ϕa		CMOS logic compatible. Negative logic. Binary code input pulses to select the photodiode signal. 9 bit input is required for 512 elements and 10 bit input for 1024 elements. $\overline{A0}$ is the lowest bit.
Input	Clock Pulse $\phi 1$, $\phi 2$, $\phi 3$		CMOS logic compatible. Positive logic. For driving the decoder in the MOS image sensor and also for processing the data video. Maximum frequency 62.5 kHz.
Input	Clock Pulse $\overline{\phi 1}$, $\overline{\phi 2}$		CMOS logic compatible. Negative logic. For cancelling the switching noise that can be accompanied with $\phi 1$ and $\phi 2$ in the signal processing section.
Output	Monitor Video	M.V.	Positive output. This is the integrated video signal from the MOS image sensor, and used for monitoring when cancelling switching noise.
Output	Data Video	D.V.	Positive output. This is the integrated, low-noise video signal from the MOS image sensor.

Figure 1: Dimensional Outline and Terminals

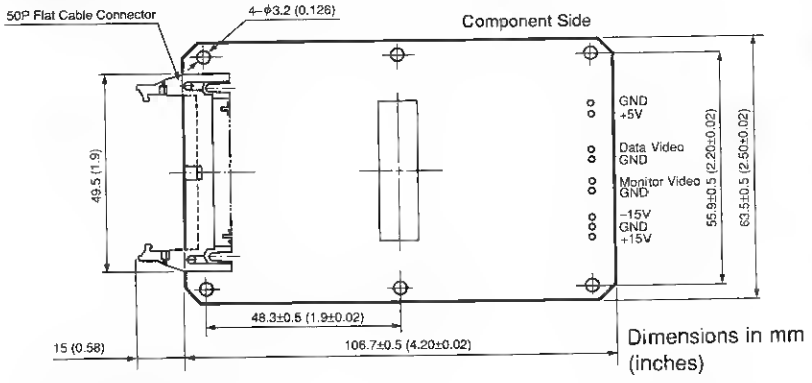


Figure 2: Wiring Example

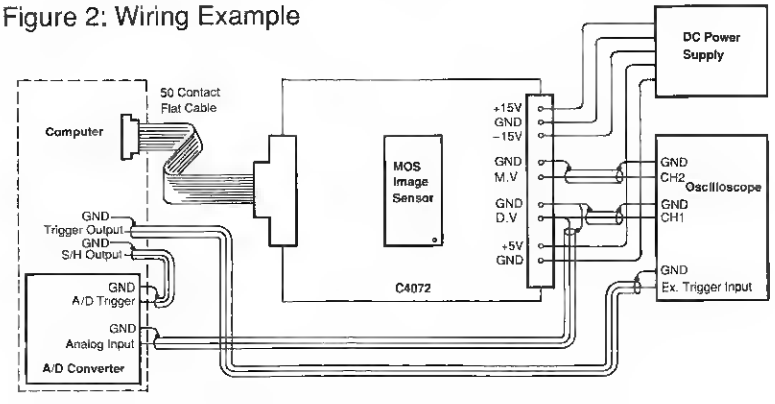


Table 1: Pin Arrangement of Flat Cable Connector

Pin No.	Function	Pin No.	Function
1-16	GND	34	GND
17	$\phi 2$	35	$\overline{A6}$
18-20	GND	36	GND
21	$\overline{\phi 2}$	37	$\overline{A5}$
22	GND	38	GND
23	$\overline{\phi 1}$	39	$\overline{A4}$
24	GND	40	GND
25	$\phi 3$	41	$\overline{A3}$
26	GND	42	GND
27	$\phi 1$	43	$\overline{A2}$
28	GND	44	GND
29	$\overline{A9}$	45	$\overline{A1}$
30	GND	46	GND
31	$\overline{A8}$	47	$\overline{A0}$
32	GND	48-50	GND
33	$\overline{A7}$		

The C4072 is supplied with a connectored flat cable (50 contacts) that can be simply interfaced with other apparatus.

Figure 3: Block Diagram

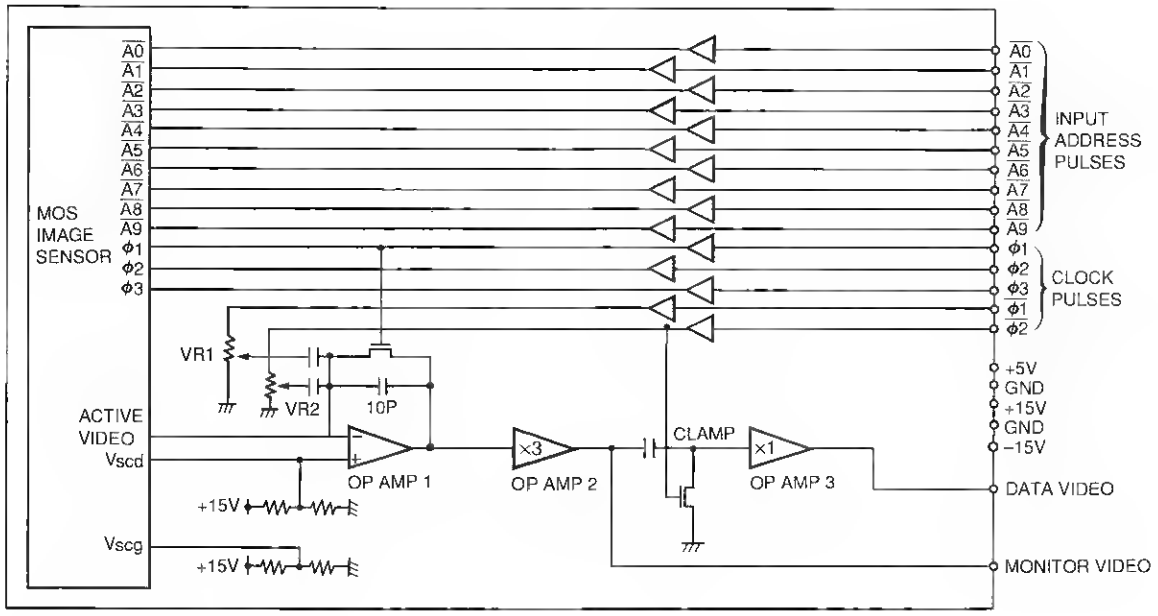
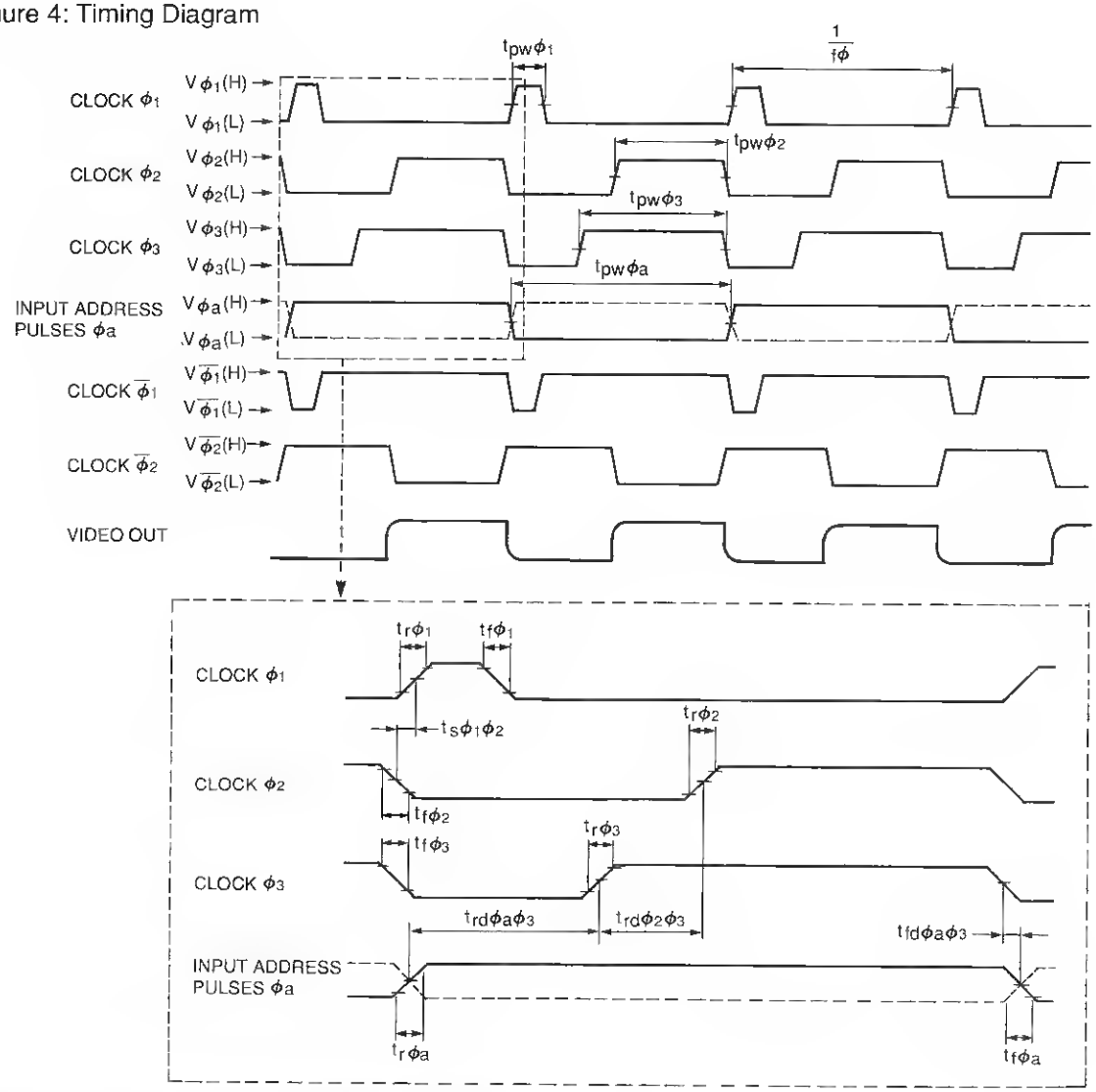


Figure 4: Timing Diagram



HAMAMATSU

TECHNICAL DATA

DRIVER/AMPLIFIER CIRCUIT C4074

For Serial/Voltage Output Type MOS Linear Image Sensors

The C4074 is a driver/amplifier circuit designed specifically for use with the serial/voltage output type MOS linear image sensors (S3921, S3924, S3922, S3923 series). The C4074 driver/amplifier circuit is simply constructed because the video-line integration in the MOS linear image sensors provides output signal with boxcar waveform. The C4074 includes a generator for the start pulse and two-phase clock pulses used to drive a MOS linear image sensor and an amplifier used to read out the video signal. The signal inputs required for the C4074 are only a master start pulse, master clock pulse, and +5V and ±15V.

In addition, the C4091 pulse generator is available, which supplies the C4074 with a master start pulse and a master clock pulse.

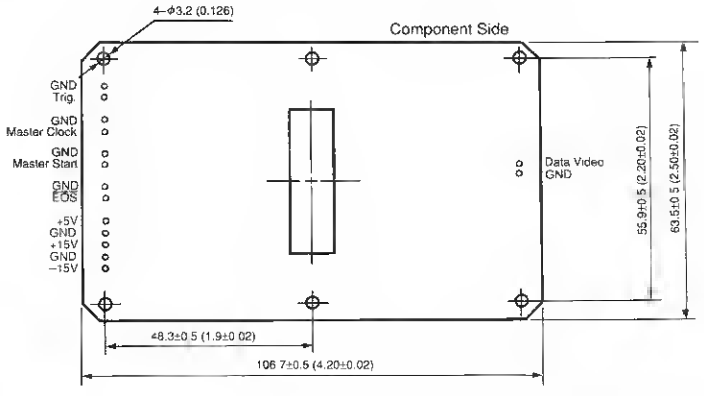
FEATURES

- **Structure allows easy cooling and optical alignment of MOS image sensor.**
- **Simple operation: only a master start pulse, a master clock pulse, +5V and ±15V required**
- **Low cost**
- **Wide dynamic range**
- **Simple adjustment**

DESCRIPTIONS OF TERMINALS

	Terminals	Symbols	Descriptions
Input	Supply Voltage	V_d (+5) V_a (+15) (−15)	+5 Vdc, 70 mA +15 Vdc, 20 mA −15 Vdc, 20 mA
Input	Master Start ϕms	St.	CMOS logic compatible. Positive logic. For initializing the circuit and the MOS shift register.
Input	Master Clock ϕmc	CLK	CMOS logic compatible. The maximum frequency 3 MHz. For synchronizing the circuit and the MOS shift register.
Output	Data Video	Video	Positive polarity output. This is the amplified video output of the MOS image sensor, with the polarity reversed and the DC offset cancelled.
Output	Sample-and-hold	Trig.	CMOS logic compatible. Positive logic. This output is used for the trigger signal for the sample-and-hold and A/D conversion.
Output	End of Scan	$\overline{EOS}$	CMOS logic compatible. Negative logic. This is the end-of-scan signal of the MOS shift register and obtained being synchronized with the ϕ2 timing right after the last element is scanned.

Figure 1: Dimensional Outline and Terminals



Dimensions in mm (inches)

Figure 2: Wiring Example

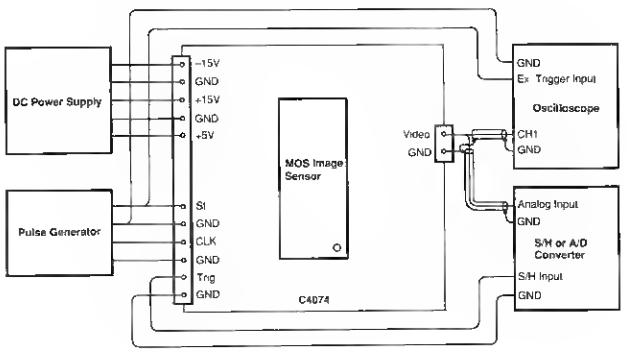


Figure 3: Block Diagram

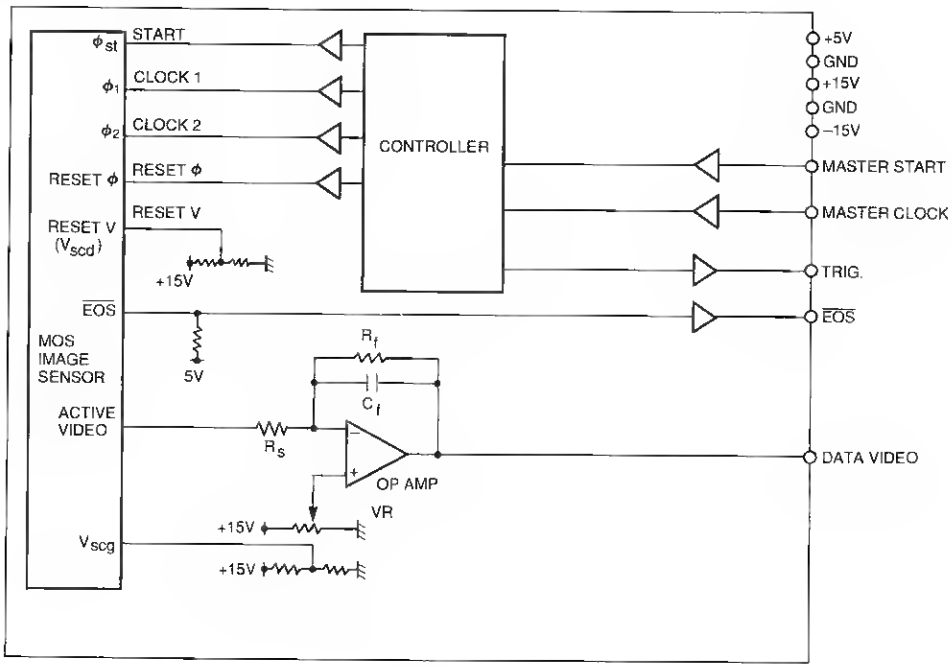
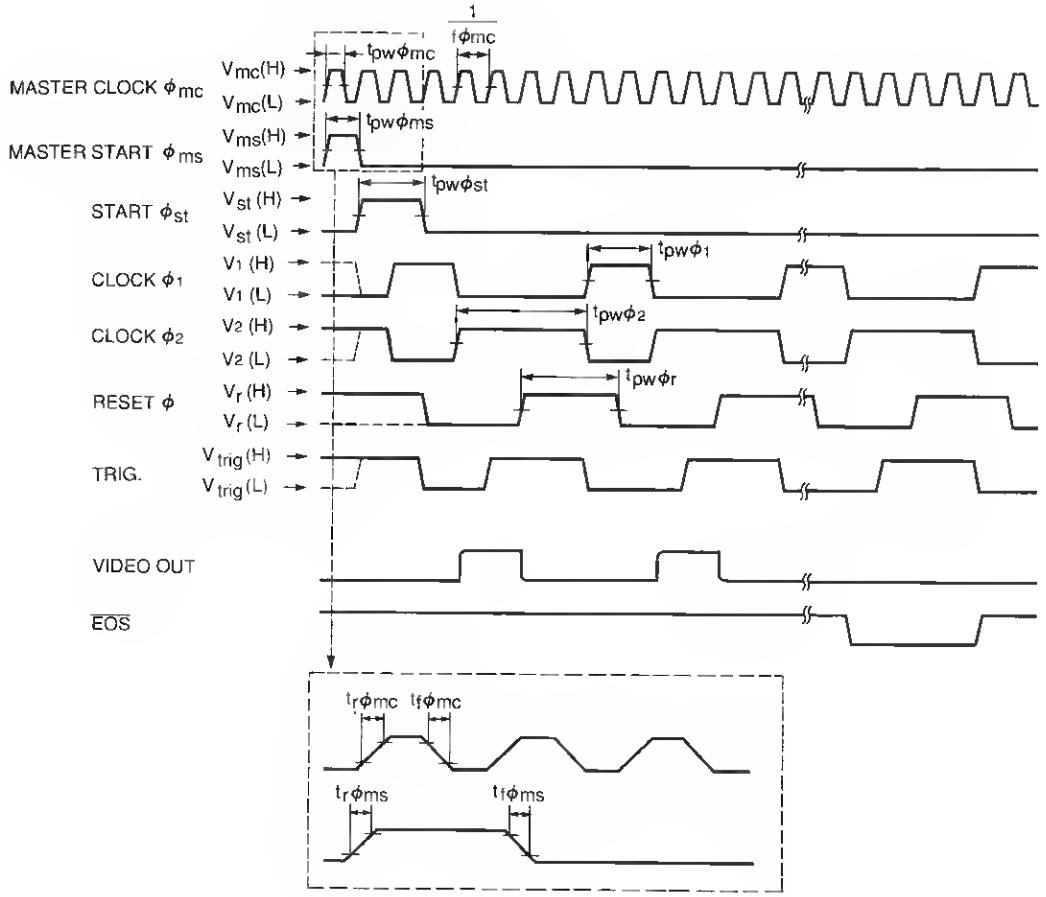


Figure 4: Timing Diagram



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